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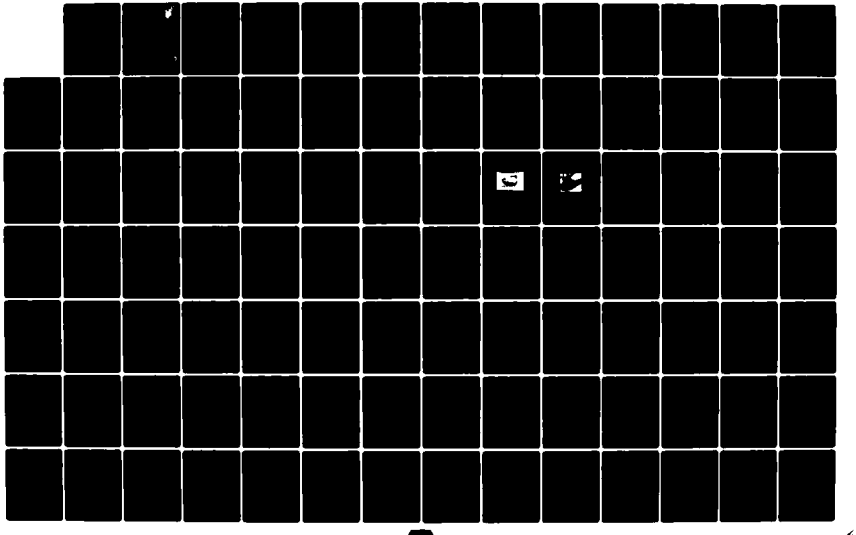

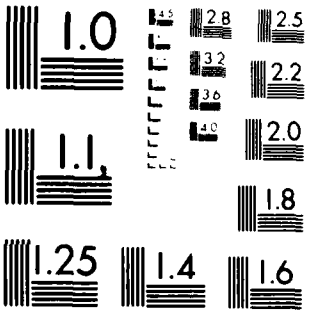

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March 1983

APPLICATION GUIDELINES FOR QUALITY ASSURANCE PROCEDURES FOR HYBRID MICROCIRCUITS

The Singer Company

G. H. Ebel, J. A. Jeffery, H. A. Engleke, B. D. Ossenkopp and D. J. Glick

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ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, NY 13441

APPLICATION GUIDELINES FOR QUALITY ASSURANCE PROCEDURES FOR HYBRID MICROCIRCUITS

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RADC-TR-83-74 has been reviewed and is approved for publication.

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The objective of this effort was to generate a complete package of documentation to define Quality Assurance Procedures for Hybrid Microcircuits. Implementation of these documents should result in reliable, cost effective hybrids for use in government equipment. The very nature of hybrids makes the generation of standard documents a difficult task since no two hybrid microcircuit suppliers use the same approach, materials, processes or procedures. The documents developed during this contract attempt to cover

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most cases that occur in the hybrid microcircuit industry today. The focus was on how to evaluate processes based on the physics of the situation, rather than directing those to be used.

The major documentation generated or updated during this effort are:

a. Test Method 2017 of MIL-STD-883
b. Test Method 5008 of MIL-STD-883
c. Appendix G of MIL-M-38510
d. Baseline Requirements
    1. Line Certification
    2. Fabrication Techniques and Material Qualification Procedures
    3. Design Guidelines
e. Application Guidelines.

Items a through c are updates of existing documents. S level requirements have been included in these documents. They have been fully coordinated and incorporated into the latest versions of MIL-STD-883 and MIL-M-38510. Item d is a new document that will be coordinated with industry and the services. This document has been circulated to the JEDEC committee 13.5 for review. Item e is also a new document and forms the major portion of this final report.

The most significant changes to items a through c are summarized in this report. Also, the highlights of the new documents incorporated in the Baseline Requirements are discussed in the summary. The application guidelines contained in this report discusses current hybrid problems. The problems are briefly outlined and the physics of the situation is discussed Recommendations for possible solutions or further effort required are presented.

EVALUATION

The objective of this effort which supports RADC TPO 4F.1 Solid State Device Reliability was to revise the appropriate sections of MIL-M-38510, "General Specification for Microcircuits" and MIL-STD-883, "Test Methods and Procedures for Microelectronics" to make them applicable to state-of-the-art hybrid microcircuits. This study has developed a compatible approach for selecting and testing high cost low volume custom hybrid microcircuits. The documentation package described includes stringent general requirements and detailed product assurance testing. These new procedures are considered unique because they require the audit and certification of hybrid manufacturer's lines and facilities by a government representative prior to supplying nonstandard parts for military systems. Testing to be performed includes both inprocess tests and controls, screening, quality conformance testing and design verification or margin assessment. Minimum acceptable hybrid microcircuit design guidelines will also be published in the near future. It is recommended that the complete package consisting of Appendix G to M38510, "General Requirements for Custom Hybrid Microcircuits," Method 5008 of MIL-STD-883, "Test Procedures for Hybrid and Multichip Microcircuits" and MIL-STD-1772 "Certification Requirements for Hybrid Microcircuits Facilities and Lines" and the applicable design guidelines be used in order to achieve the desired device reliability. Appendices A and B of this report illustrate the approach contained in a user company's general and detail specifications to implement the aforementioned documentation, test and control required to procure and test hybrid microcircuits for military systems.

John P. Farrell

JOHN P. FARRELL
Project Engineer

PREFACE

Throughout the effort associated with the performance of this contract, a large number of individuals in the hybrid microcircuit field were generous contributors in many ways. The JC 13.5 committee under the direction of Mr. Jim Estep worked constructively to develop the upgraded versions of MIL-STD-883 and MIL-M-38510. Mr. Giles Massie and Mr. Sid Eichel from Teledyne coordinated changes to Test Method 5008, and Mr. Donald Weinstein of CTI coordinated Test Method 2017. Mr. Dan Epstein did the work on Appendix G of MIL-M-38510. The following is a list of other contributors that should be acknowledged.

a. For general comments and review:

- Harry Bonham, Rockwell International
- Philip Eisenberg, Northrup Corporation
- Jerry Fischel and staff, CTI
- John Forster, Singer Kearfott
- Richard Gerber, Aerospace Corporation
- James Mason, General Electric
- John Ousta, Singer Kearfott
- Isaac Pratt, U.S. Army, ERADCOM
- Ralph Redemske, Teledyne
- Charles Totten, Rockwell International
- Hoyle Yearwood, NASA/Marshall

b. For polymer adhesives:

- Phillipp wh Schuessler, IBM

c. For particle getters:

- o Richard Dinsmore, Beckman
- o Len Marro, CTI

d. For thick film resistor qualification:

- o David Zarnow, U.S. Navy, NAC Indianapolis

e. For subtrate attachment qualification:

- o Kent Harmisson, U.S. Navy, NAC Indianapolis

f. For the line certification audit:

- o Frank Meccia and W. Macre, Singer Kearfott

g. For preparing sample procurement drawings:

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Particular acknowledgement should be made here for the advice, assistance, encouragement and patience of Mr. John Farrell throughout the program.

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1. INTRODUCTION

1.1 General. The usage, quantities and complexity of hybrid microcircuits in military systems is steadily increasing. However, the procedures and processes by which these devices are constructed, selected and tested vary greatly due to a lack of standardization in the hybrid microcircuit industry and because of the various technologies and materials used in their fabrication.

Early hybrid microcircuits were designed to be used for those system functions that were highly repetitious such as amplifiers, switches, choppers etc. The recent trend has been to design more complex hybrids which, in effect, replaced printed circuit boards on a one-for-one basis. These hybrids typically contain from 15 to 45 active devices and from 300 to 600 interconnecting wires. The rapid use of these complex hybrids in military systems necessitated a new look at standardization of quality assurance procedures.

The first attempt to standardize hybrid microcircuit testing was the generation and issuance of Test Methods 5008 and 2017 of MIL-STD-883 and Appendix G of MIL-M-38510 for procurement of hybrid microcircuits. Various research efforts in DoD and NASA have provided many documents to aid in determinining acceptable hybrid fabrication techniques, materials and test procedures. This program made use of these documents to evaluate and consolidate these efforts, existing DoD hybrid microcircuit standards, JEDEC committee activities and other industry efforts in these areas, to generate a complete procedure to be used in approving Class B and Class S hybrid microcircuits for DoD and NASA use.

1.2 Objective. The main objective of this program was to

develop the documentation to test Class B and Class S thick and thin film hybrid microcircuits, including microstrip and stripline technologies, in an efficient, economical and timely manner. Efficient in the sense that design guidelines and line certification should reflect processes that will result in better than 90 percent yield. Poor yields create both higher costs and lower reliability. Economy must be considered from the life cycle costing aspect. Consideration of all technologies that will probably be used for the next 10 years must be included for this program to be timely.

2. GENERAL

2.1 Summary of documents generated. As a result of a contract with Rome Air Development Center (F30602-79-C-0181), the following list of documents defining "Quality Assurance Procedures for Hybrid Microcircuits" have been generated or updated:

a. Test Method 2017 of MIL-STD-883 (Notice 5, 15 January 1982)

b. Test Method 5008 of MIL-STD-883 (Notice 5, 15 January 1982)

c. Appendix G of MIL-M-38510 (Revision E, 1 December 1981)

d. Baseline requirements

1. Line certification of fabrication processes (MIL-STD-1772) Proposed

2. Design guidelines

2.2 Contract objectives. The main objective of the RADC contract on "Quality Assurance Procedures for Hybrid Microcircuits" is to generate a set of documents that will result in reliable, cost effective hybrids for use in Goverment equipment. The very nature of hybrids makes this a difficult task since no two hybrid microcircuit suppliers use the same approach, materials or processes. The documents developed during this contract attempt to cover most cases that occur in the hybrid microcircuit industry today. The focus on this contract was on how to evaluate processes, rather than directing those to be used. The approach was three pronged as follows:

a. Revision of the day-to-day working documents contained in MIL-M-38510 and MIL-STD-883. The major emphasis here is on upgrading Test Methods 2017 and 5008 of MIL-STD-883 and Appendix G of MIL-M-38510.

b. Generate a set of baseline documents for hybrid microcircuit users to evaluate materials and processes employed by hybrid microcircuit suppliers and to assure that the necessary documentation is in place to control the consistency of the product. The major documents in this area are new and consist of line certification, fabrication techniques and material qualification, and design requirements.

c. Prepare application guidelines that would serve to tie the other documents together. It would contain sample Specification Control Drawings for both B and S level documentation (see Appendix A and B) as well as suggested methods for reliable hybrid microcircuit construction.

Some examples of changes to MIL-STD-883 and MIL-M-38510 are discussed in the following subparagraph.

2.2.1 Test Method 2017 of MIL-STD-883.

a. All spacings between conductors having different voltage levels have been increased to a minimum of 1 mil. This is to preclude shorts caused by loose particles that cannot be detected easily by loose particle testing in accordance with Test Method 2020 of MIL-STD-883.

b. The resistor trimming section has been expanded to cover the newer techniques.

c. Requirements for microwave integrated circuits (MIC's) have been added to the test method.

d. A criteria has been added to cover the spacing between a lead wire and the exposed silicon at the edge of a chip.

e. Compound bonds have been defined and limitations specified. A compound bond is the monometallic bonding of one bond on top of another. With the advent of plasma cleaning of hybrids prior to wirebonding, it has become almost impossible to remove a wire from a semiconductor device without pulling out some silicon. Therefore, any miswire required the replacement of that semiconductor device. The use of compound bonds made such rework events less difficult and more reliable. Tests run independently in several locations showed compound bonds to be reliable if the limitations called out in paragraph 3.1.6.5. of Test Method 2017 are followed. Since compound bonds are monometallic, nondestructive bond pull tests of each compound bond should be all the testing that is required to control the reliability of these bonds.

f. Class S requirements have been added.

2.2.2 Test Method 5008 of MIL-STD-883.

a. This test method has been reformatted to eliminate confusing footnotes.

b. A 300°C preconditioning test has been added to the Group B wirebonding tests to control detrimental intermetallic formation.

c. Except for class S parts, wirebond tests have been eliminated from the 100 percent screening tests in favor of in-process verification.

d. Based on the increased spacing required in Test Method 2017 of MIL-STD-883, the particle impact noise testing has been removed from Class B devices.

e. All the testing that can be accomplished at the package manufacturer has been put in the Group D testing to assure that defective packages can be screened out of the system economically and early in the build cycle.

f. Class S requirements have been added.

2.2.3 Appendix G of MIL-M-38510. This is basically a new document that is more comprehensive than the present Appendix G. The major reason for the change is to make the document easier to use by concentrating the major requirements for hybrids in one document. From a technical standpoint, some of the more significant additions are:

a. Incorporation of definitions and concepts for both rework and repair.

b. Section on rework/repair has been expanded.

c. One delid/reseal cycle is allowed for an approved and qualified process.

d. Class S requirements have been added.

2.2.4 Baseline requirements.

2.2.4.1 Line certification of fabrication processes (MIL-STD-1772). The purpose for MIL-STD-1772 (Produce Assurance Provisions for Custom Hybrid Microcircuits-Line Certification of Fabrication Processes) is to provide a uniform method for evaluating materials and processes for hybrids and to assure that the processes being certified will result in satisfactory product throughout its useful life. This document is not intended to direct or select the use of any particular material or process but only to standardize on the minimum testing required to certify a process and the documentation required to assure that this certified procedure will continue to generate satisfactory products.

MIL-STD-1772 is intended to standardize the documentation and testing for hybrid microcircuits for use in military and aerospace applications. It covers the interface between user and manufacturer and it is not intended to be a complete set of documentation required to build hybrid microcircuits.

Standardization of the interface requirements between user and manufacturer will be beneficial to both parties. Since this standard qualifies processes rather than specific hybrids, the amount of testing can be held to a minimum. Once the process is qualified to the standard, little or no additional testing would be required unless the process changed significantly. All users will be able to use the same test data thus saving both time and money.

The audit program will require a little more effort since this is repeated annually (except for Internal Visual, Wirebonding and Package Sealing which are audited semiannually). One of the prime reasons for the audit is to assure a good communication channel between the user and manufacturer. By standardizing the

audit, the burden on both the user and manufacturer should be reduced.

The new versions of MIL-STD-883 and MIL-M-38510 reduced certain requirements based on compliance with MIL-STD-1772. This was done to move some controls from the area of screen testing to the area of line process control. By doing this, the overall hybrid manufacturing efficiency will be improved by having the controls earlier in the manufacturing cycle. Some examples of this are detailed as follows:

a. Centrifuge - The requirement for centrifuge screen testing was reduced from 10Kg to 5Kg. However, the process qualification requires levels to 20Kg (package bottom stiffeners are allowed to prevent erroneous results for "oil canning"). A series of tests on many hybrids showed the substrate and component attachment procedure could routinely pass the 20Kg test. This then provides a good safety margin between the 5Kg screening requirement and actual process capability.

b. Delidding and Resealing - One delid/reseal cycle is now allowed based on the assumption that the process was qualified to MIL-STD-1772.

c. PIND Testing - For B level parts PIND testing has been eliminated in favor of line sampling and corrective action.

d. Wirebonding - Most of the wirebond testing during screening (only Group B testing is required) has been removed in favor of in process qualification to MIL-STD-1772.

2.2.4.2 Design guidelines. The design requirements document will list those design practices that are considered necessary by most hybrid microcircuit suppliers to produce high quality, reliable hybrids. It contains those items listed on most internal design guidelines in current use by hybrid microcircuit suppliers. The guidelines selected for this document are those involving the user and supplier rather than the detailed design guidelines which are unique to special construction methods.

2.3 Discussion of B and S level requirements. The documents generated during this contract cover both B and S level hybrid microcircuits. The differences between the two levels are detailed in Test Methods 2017 and 5008 of MIL-STD-883 and Appendix G of MIL-M-38510.

2.4 Package sizes. Except where specifically noted in Test Method 5008 of MIL-STD-883, the documents generated under this contract apply to all sizes of packages and include the following hermeticaly sealed hybrid microcircuit package types:

a. Flat pack types utilizing metallized film conductors.

b. Flat pack types utilizing individual glass to metal seal conductors.

c. Flat pack types utilizing lead frame conductors.

2.5 DoD and NAS agencies. Personnel from the following DoD and NASA Agencies were contacted for suggestions and information concerning the generation of the documents included in this contract:

USAERADCOM
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MIRADCOM
DRDMI
Redstone Arsenal, Ala 35809

Naval Ocean Systems Center
Code 9253
San Diego, CA 92152

Naval Air Systems Command
Code--Air--52022F
Washington, D.C. 20361

NASA
Marshall Space Flight Center
Huntsville, Ala 35813

NASA
Lyndon B. Johnson Space Center
Code--ED--73
Houston, Tex 77058

Naval Avionics Facility
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Indianapolis, Ind 46218

Crane Naval Weapons Support Center
Code 7024 Bld 2906
Crane, Ind. 47522

3. DISCUSSIONS AND RECOMMENDATIONS FOR IMPROVING CURRENT HYBRID PROBLEMS

3.1 General. In this section, current hybrid problems are discussed. The problems are briefly outlined and the physics of the situation is discussed. Recommendations for possible solutions or further effort required are presented.

The items discussed in this section are not intended to cover all of the present hybrid problems. They are the major items that kept surfacing during discussions with hybrid suppliers and users as well as government representatives responsible for hybrids.

3.2 Wirebonding. Historically, wirebonding has been ranked prominently in most studies of hybrid microcircuit failures. With the advent of better wirebonding equipment, better controls, and a better understanding of the major failure mechanisms, many recent studies have shown a decline in wirebonding failures.

The gold/aluminum intermetallic interface has traditionally been responsible for most of the long term bond failures in hybrids. There are two mechanisms associated with this phenomena. One has to do with insufficient energy being used to make the bond. This mechanism results in a process with an activation energy of about 1.0 electron volts. The other mechanism results from contaminates in the interface and results in a process with an activation energy of about 0.4 electron volts. Both failure mechanisms can easily be detected using a one hour bake at 300^{o}C. For this reason, Group B testing of MIL-STD-883, Test Method 5008, now requires gold/aluminum bonds to be preconditioned at 300^{o}C for one hour prior to pull testing. For the case of aluminum wire to gold pads, Okumura has shown the gold thickness

must be considered before high temperature acceleration of wire bond failures are attempted.[1]

To eliminate failures caused by insufficient energy in making the bond, a certain amount of care and testing is required. Large silicon chips have different thermal characteristics than small ones. Eutectic versus organic chip bonding also affects the thermal characteristics of the bonding process. For example, if a bond schedule is set so that a polymerically attached integrated circuit results in good intermetallic properties, then bonding to small eutectically attached diodes may present a problem. The thermal impedance of the diode would be considerably less than that of the integrated circuit and could easily result in not enough energy being available at the bond interface to produce an adequate bond. Therefore, in setting up bonding schedules consideration should be given to such things as:

- Die size
- Die attachment material
- Bond interface temperature
- Ultrasonic power (if used)
- Bond tool pressure

---

[1]Okumura, K., "Degradation of Bonding Strength (Al Wire-Au Film) by Kirkendall Voids", Journal Electrochemical Society: Solid-State Science and Technology, March 1981, pp. 571-575.

Care must also be taken so that the silicon beneath the bonding area is not damaged resulting in latent cratering defects. When wirebonding discrete simiconductor parts, it is relatively easy to set up a bonding schedule since all the parts can be bonded using an optimum schedule. In hybrids, it would not be cost effective to wirebond each semiconductor device with its optimum bonding schedule (unless automatic bonders are used) since the number of schedules would lead to logistics problems on the production line. Fortunately, the acceptable bonding window for gold/aluminum bonds is sufficient to minimize the number of bonding schedules required. Proper design of circuits can minimize the problem by adjusting thermal impedances. The use of different wire diameters can also be used to minimize the number of bonding schedules required.

Before release of bonding schedules are made for production hybrids, the effect of high temperature (300^{o}C) testing should be evaluated. Possible cratering caused by improper bonding pressures or ultrasonic energy levels should also be evaluated. In order to detect cratering, the metalization must be removed from the bonding pad area. A quantitative method of evaluating the wirebonding process will be discussed later in this section.

The intermetallics formed in the bond interface, when contamination is present, has a much lower activation energy than the normal bonding process. If the high temperature (300^{o}C) testing results in bond failures, then it is a relatively simple matter to determine if the process has a high or low activation energy and thus determine the area in which to initiate corrective action. Argon plasma cleaning has been demonstrated to be extremely beneficial in improving intermetallic problems in general, and contamination problems specifically. This subject is discussed in more detail in the section on plasma cleaning.

Generally, wirebond pull strength data from hybrids is difficult to interpret in the tabular form in which it usually appears. Not all of the data points are used in making decisions. The low bond strength values or failure points receive most of the attention. The process mean, and sometimes the standard deviation, is usually all of the statistical data contained in the summary reports. Attempts to use $\bar{X}$ and R (mean and range) charts to control the wirebonding process have generally been ineffective.

The statistical approach summarized here was developed in 1914 by Hazen.[2] It is one of the most valuable tools for graphical statistical analysis of normally distributed variables. Hazen developed probability paper which plots the variable value against the standard deviation or probability of occurrance. For normal distributions, plots made on probability paper result in a straight line. Wirebond strength data from a well controlled process will result in a plot having a single straight line.

More than one straight line indicates several processes at work and a single point well off of the straight line would indicate a "sport". Using this technique, all of the data is available on one graph so that intelligent decisions can easily be made as to what action should take place to improve a process.

To initiate the statistical method, an Apple II Plus desktop computer was interfaced to a Unitek Micropull III wire loop pull tester. A computer program was then written to input the information from the Unitek. The object of the program was to minimize throughput of the Unitek. An external keypad adjacent to the pull tester facilitates operator entry of the failure codes and other information.

---

[2]Hill, L. R. and Schmidt, P. L., "Graphical Statistics - An Engineering Approach", Westinghouse Engineer, March 1950.

The initial information concerning the test device is fed into the computer by the operator. The program is then set-up to automatically sequence through the wire numbers. The operator has only to pull the wires in sequence and key in a failure code. The wire number, pull strength and failure code are printed. The coding is designed to provide some flexibility. There are special codes which allow the sequencing to be reversed or advanced when needed.

When all the wires have been pulled, the analysis begins. The data is sorted in order of increasing magnitude. A value is then computed for each point based upon its cumulative percentage. The points are then compared with an array containing values that represent the normal curve. Based on these comparisons, an abscissa value is determined. This information is stored as a coordinate system for use by graphing programs.

Graphical analysis begins by performing a least squares on the data to find the slope of the line. The slope is then extrapolated back to determine the point that the line intersects the abscissa. This point is the zero break force point. The value of sigma at the zero break force point is used to predict the probable number of failures in that bonding run. How closely the data forms a straight line denotes its adherence to the normal distribution.

The particular program used at present (see Appendix C) also computes the coefficient of determination which is a figure that denotes a percentage of adherence of the least squares to the data. After this information has been obtained, the data is automatically printed on standard reliability paper. The next step in the program will be to automatically plot the confidence intervals.

A few examples of actual situations and the corrective action taken should serve to show the effectiveness of this approach to wirebonding evaluation. The details of the procedure along with a sample program written in basic computer language is contained in Appendix TBD. The equipment required to take raw wirebonding data and produce a plot on probability paper is minimal. Any wirebond puller with digital output that can be interfaced to a small (48K memory) computer is all that is required.

Figure 1 shows the results of a bond pull test on a hybrid containing 209 gold to aluminum wire bonds. The part was conditioned at 300^{o}C (in dry nitrogen) for 4 hours before the bonds were pulled. The ordinate scale is bond strengths in grams and the abscissa scale is standard deviation. It is obvious that the data does not fall in one straight line but in three distinct lines. The line of small dots shows the "least square" fit for all 209 points. When a such situation occurs, it indicates that three processes are present. The first set of 15 points forming the first straight line (-3.0 to -1.8 sigma) were all ball lifts.

The set of 18 points forming the second straight line (-1.8 to -1.3 sigma) were all heel breaks of gold wire on thick film gold. This failure mechanism now appears to be the most prevalent in hybrids that have been manufactured on lines where the intermetallics (both contamination and energy) problems have been corrected. The remaining 176 points form the third straight line and is representative of the standard production process. If the data is seperated so that individual processes can be evaluated separately, then some conclusions can be made based on sound statistical data.

Figure 2 shows the plot of the 15 ball lifts. This plot is a straight line intersecting the abscissa at -1.76 sigma. Therefore, the probability of success for each bond, for the process resulting in lifted bonds, is only about 96 percent. Or stated differently, four out of every hundred bonds from this

DESTRUCTIVE BOND PULL TEST
SKD COMPONENTS LAB

PART NUMBER - 2271430
LOT IDENTIFIER - S/N 5424
NAME - JEFFERY
DATE - 6-23-81
WIRE - 1 MIL GOLD TO ALUMINUM
SPECIAL CONDITIONS - 300 C NITROGEN BAKE FOR 4 HRS

THE MEAN =7.079
STANDARD DEVIATION =2.357
% STANDARD DEVIATION =235.70
NUMBER OF BONDS PULLED =209
NUMBER OF FAILURES = 15
MIN ALLOWABLE BOND STRENGTH = 1.25
ZERO CROSSING AT 3.22 SIGMA
COEFFICIENT OF DETERMINATION IS .797
COEFFICIENT OF CORRELATION IS .893

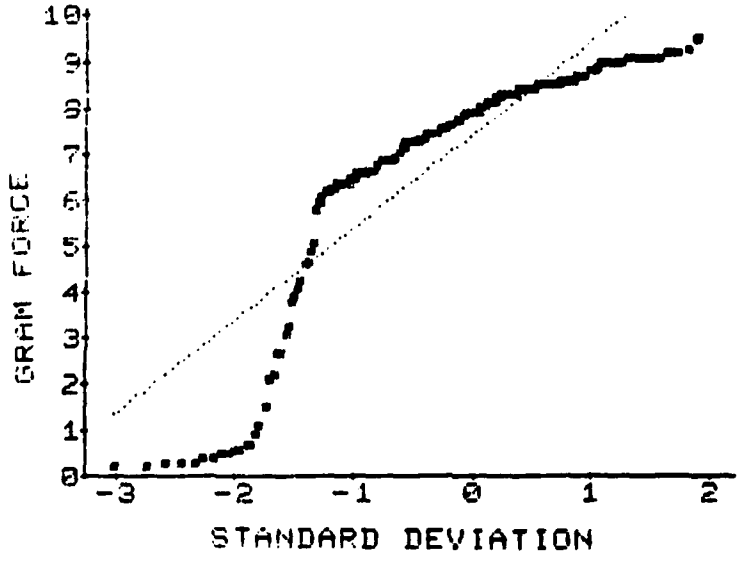

FIGURE 1. PROBABILITY PLOT SHOWING THREE DISTINCT MECHANISMS

ZERO CROSSING AT 1.76 SIGMA
COEFFICIENT OF DETERMINATION IS .931
COEFFICIENT OF CORRELATION IS .965

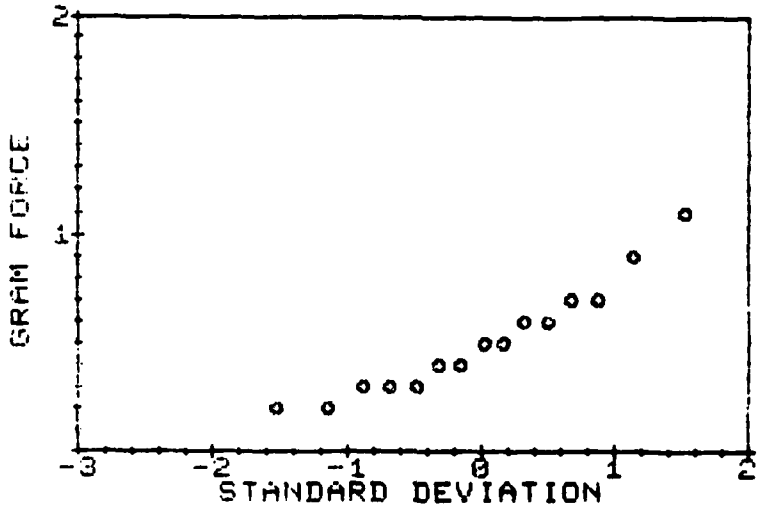

FIGURE 2. PROBABILITY PLOT SHOWING
TWELVE BOND LIFT FAILURES

distribution will result in a failure.

Figure 3 shows the plot of the 18 heel breaks. This plot intersects the abscissa at -2.54 sigma which indicates a probability of success, per bond, of only 99.4 percent. The remaining set of 176 data points representing the main process distribution resulted in a plot that intersected the abscissa beyond -6 sigma indicating less than one failure per billion bonds.

The analysis gathered from this study result in some interesting conclusions not obtained by the methods generally used to evaluate wirebonds for military hybrids. A look at the data shows an excellent basic process. Corrective action that would eliminate heel breaks and ball lifts without significantly affecting the basic process would result in an excellent process. An investigation of the ball lifts showed them to be concentrated on two adjacent integrated circuits. Some surface contamination was noted in the general area of these integrated circuits. This suggests that the ball lift mechanism could be eliminated by better surface cleaning (such as plasma) just prior to the wirebonding operation. The plasma cleaning would also allow the bonding pressure to be reduced for the heel bonds thus removing that failure mechanism.

After the suggested changes were made to the bonding processes, a second sample was run through the same tests as above. This time, the sample of 250 gold wires on aluminum metallization resulted in the plot shown in Figure 4. This process resulted in a zero bond strength greater than -6.6 sigma, or better than one in a billion failures.

Another interesting aspect of this example is that the only failures were bond lifts and yet, considering the preconditioning, it would seem more probable that a heel break would be the more likely failure mechanism. That would certainly be true of the

ZERO CROSSING AT 2.54 SIGMA
COEFFICIENT OF DETERMINATION IS .983
COEFFICIENT OF CORRELATION IS .991

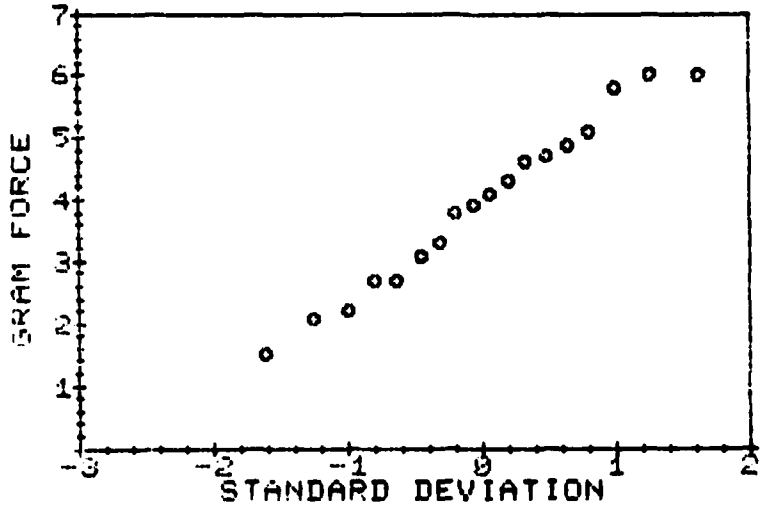

FIGURE 3. PROBABILITY PLOT SHOWING EIGHTEEN HEEL BREAK FAILURES

ZERO CROSSING AT 6.66 SIGMA
COEFFICIENT OF DETERMINATION IS .988
COEFFICIENT OF CORRELATION IS .994

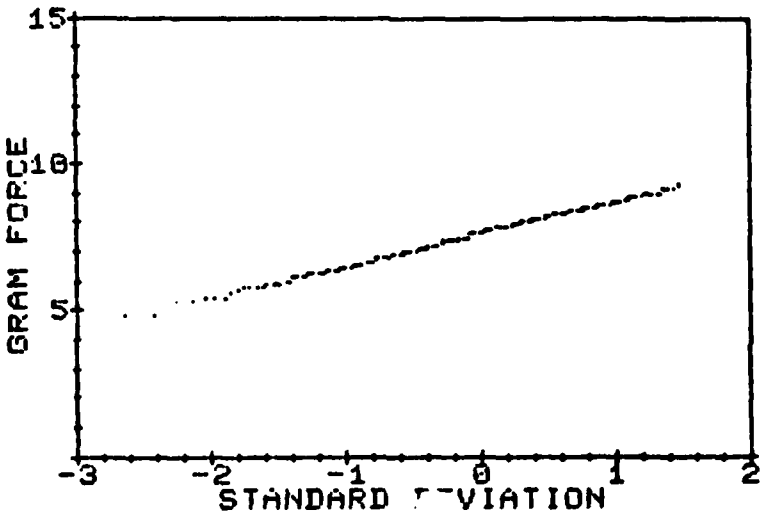

FIGURE 4. PROBABILITY PLOT SHOWING RESULTS OF CORRECTIVE ACTION

failures during the first year or two of operation. Based on the present testing methods, the part would have passed on the heel break mechanism alone (excluding ball lifts) and yet the statistics would indicate that the possiblity of a heel break is rather high. If we assume a probability of success of 99.4 percent, and 18 bonds with this mechanism in each hybrid, then about one out of every eight hybrids would fail due to a heel break.

Another example of the value of using probability paper to investigate bond quality is a case where a single failure occurs during a test. The following example explores the action taken in two cases each of which had a single bond failure. Figure 5 shows a plot of bond pull data from manufacturer A. The single failure point falls slightly off a straight line drawn through the rest of the data points. The failure mechanism was a ball lift. Since the rest of the data indicated a zero bond strength level at only about -2.7 sigma (99.7 probability of success for a given wirebond), the lot was rejected. The data in this case showed the basic wirebonding process needed improvement.

In the case of manufacturer B, the situation is different. Figure 6 shows the plot of the data from a wirebond test on manufacturer B. The failure point lies well off of the straight line determined by the rest of the data points. The mechanism of failure was again a ball lift. In this case, however, it was not caused by intermetallic formation but by "cracking" in the bulk silicon. Figure 7 shows the bond pad location and Figure 8 shows a side view of the lifted bondwire.

Clearly a large chunk of silicon was removed with wire. The main process, in this case, shows a zero bond strength at about 4.8 sigma (99.99992% probability of success for a given wirebond). The results in this case show the lot to be acceptable but not

THE MEAN =6.57
STANDARD DEVIATION =2.31
% STANDARD DEVIATION =231.74
NUMBER OF BONDS PULLED =70

NUMBER OF FAILURES = 1
MIN ALLOWABLE BOND STRENGTH = 2.5

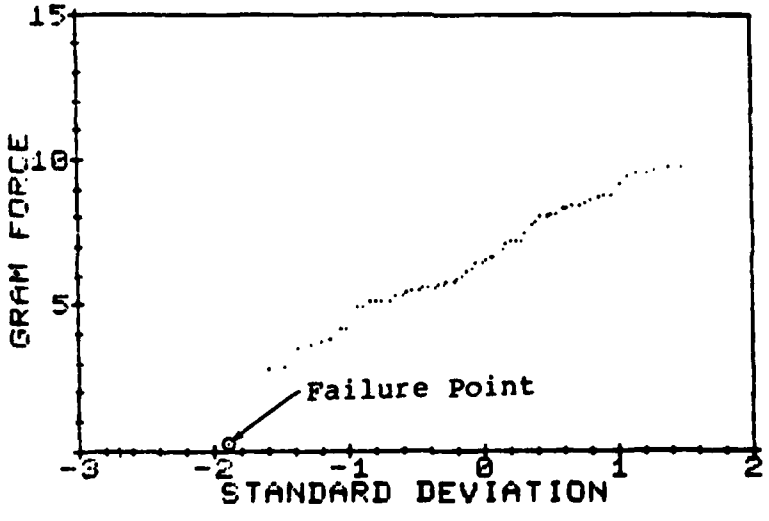

FIGURE 5. PROBABILITY PLOT SHOWING DATA FROM MANUFACTURER A

THE MEAN =7.08
STANDARD DEVIATION =1.53
% STANDARD DEVIATION =153.78
NUMBER OF BONDS PULLED =142

NUMBER OF FAILURES = 1
MIN ALLOWABLE BOND STRENGTH = 2.5

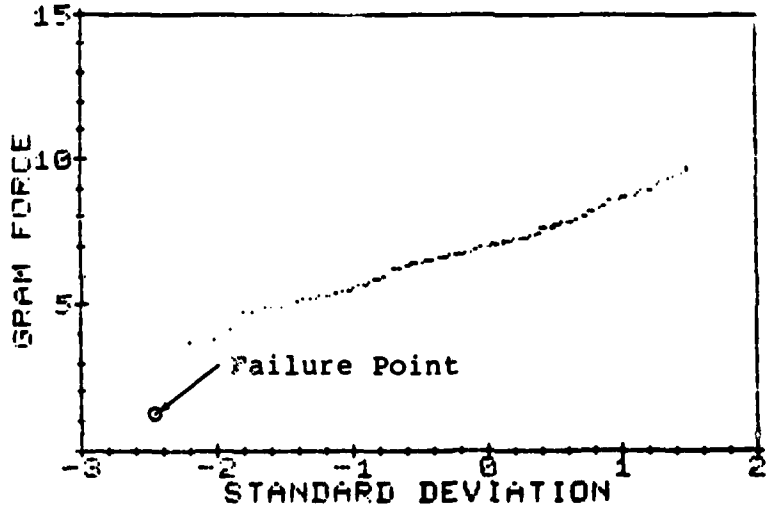

FIGURE 6. PROBABILITY PLOT SHOWING DATA FROM MANUFACTURER B

FIGURE 7. BOND PAD SHOWING SILICON PIT

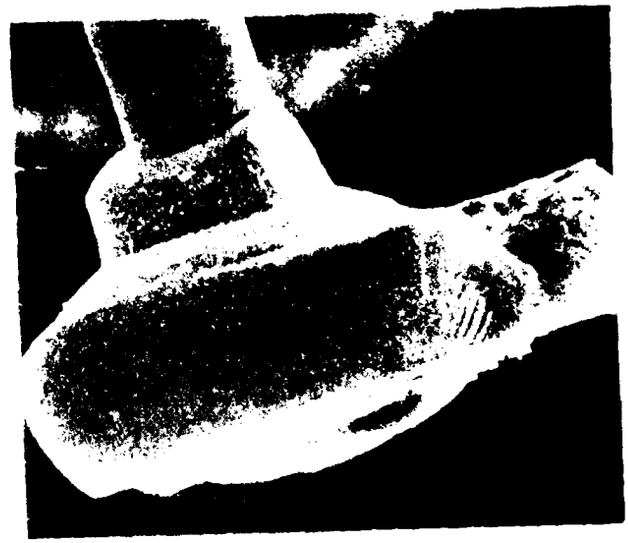

FIGURE 8. BOND WIRE SHOWING ATTACHED SILICON

excellent. Although the main process is acceptable, care should be taken to determine if the one bond failure was because of a poor silicon chip or due to process problems.

Many process controls on wirebonding can easily be evaluated using this process. With relatively few bonds, the difference between two processes can be evaluated.

3.3 Loose particle testing. As a result of increasing minimum spacing between conductors in hybrids from 0.3 mils to 1.0 mil (in accordance with Test Method 2017 of MIL-STD-883), it was possible to remove the present requirements for loose particle testing (Test Method 2020 of MIL-STD-883) from Class B hybrids.

These specification changes were based on a series of tests that were run to evaluate the present method of testing. A review of field failures due to loose particles showed that these failures fell into three classes. One class consisted of small particles bridging gaps between two conducting surfaces that were less than 1 mil apart. The second class consisted of large particles, typically 10 mils or greater, that bridged gaps of 2 mils or greater. The third class consisted of small magnetic particles that lined up to short out rather large gaps such as glass beads on packages.

A series of tests were run with a set of varying gaps between adjacent conducting surfaces. A constant voltage of 30 volts (with high series impedance) was applied across the gap. The parts were sealed with a large number of conductive loose particles (primarily gold in chip, ball, wire and flake form) in them. The parts were electrically monitored for momentary shorts across the 30 volt gap while being vibrated at 50g and 60 Hz. Failures occurred rapidly (less than 1 minute) for all gap spacings up to 0.7 mils. Failures then tapered off until a 1 mil spacing was achieved. For gaps 1 mil and larger, monitoring while under

vibration caused no failures during a 6 hour period of time. Based on this testing, 1 mil minimum spacings were instituted in Test method 2017.

A review of parts that had failed the loose particle test showed that many parts were being rejected for small non-conductive particles such as lint. Other parts showed large conductive particles such as gold eutectic and wirebonding material. Detection of small particles has been where most of the controversy has arisen in the field of loose particle testing. Large particles that are easily detected should be removed from Class B hybrids. However, the present Test Method 2020 does not allow for such discrimination between particle sizes. If a test Condition C using higher threshold levels could be developed, then an efficient and cost effective test could be established for Class B devices. A recommendation for future effort is that such a test condition be established and the requirement be added to Test Method 5008 of MIL-STD-883.

The fine magnetic particles that string together to form shorts are generally the result of lapping the Kovar package prior to sealing. Extreme care must be taken in this area to remove any small particles generated by the lapping procedure. This is especially true in packages that have been delidded. A degaussing operation folowed by multiple wash cycle appears to be effective. Also, new automatic delidding equipment now on the market reduces or eliminates the need for lapping in relidded parts. Parts with this potential failure mechanism can be successfully screenedusing a 1 hour bake at 85^{o}C followed by a 1 minute 60 Hz vibration at a 20g level. During this test, the resistance between the case and leads is monitored using a high impedence ohmmeter. Also, the parts should be tapped with a nylon rod during the 1 minute vibration. The U.S. Army Missile Command at Redstone Arsenal in Alabama has recently released an excellent report, "Delidding Hybrid Microcircuit Packages" (MICO

Project No. 3438), which describes methods that will greatly reduce or eliminate the fine magnetic particle problem (MICOM MM&T Project R793438).

3.4 Subtrate attachment. The high cost of gold has forced many hybrid suppliers to abandon gold/tin subtrate attachment material for either a lead tin base solder or polymeric materials. The major problem with the lead tin based solders (usually with an additive such as silver to bring up the melting point) is one of long time crystallization resulting in weakended bonds. Most of the problems using metallic attachment methods are understood and well documented in the literature. This is not the case with polymeric attachment. Polymeric attachment has two major areas of concern. These are:

- o Outgassing
- o Time dependent mechanical strength.

Two major problems have been reported concerning outgassing. One is moisture trapped within the polymeric material that has not been properly removed prior to sealing. The second problem has to do with outgassing materials depositing on pads where wirebonds are to be attached. Plasma cleaning (see 3.7) just prior to wirebonding has cured this problem.

The time dependent mechanical strength appears to be interrelated to the outgassing phenomena. Two observers have reported time dependent stresses on parts with areas as small as 80 mils square. This effect can take several hundred hours to reach its

maximum stress. Li, Tang and Barton observed that the device was lifted by the gasses trapped under it and the die (or substrate) elevation shows a linear function dependence on die size for a given polymeric material.

Epoxy attachment procedures have been developed by Kent Harmison of the Naval Avionics Center (NAC) at Indianapolis, Indiana. By "B" staging the epoxy, detrimental gasses are not trapped beneath the substrate or large element. Substrates attached using this method have resulted in hybrid microcircuits with low moisture content and high mechanical strength of the subtrate to the case after extensive temperature testing. Therefore, it is recommended that for attaching large elements (greater than 80 x 80 mils) or substrates, careful consideration be given to the attachment process.

The major problem associated with testing substrate attachment bond strength with large hybrids is premature failure due to the "oil-canning" effect. Most hybrids can easily withstand a 20Kg centrifuge test if a stiffener plate is added to the back of the hybrid being tested. This stiffener plate can be attached with such materials as epoxy, Eastman 910, or polyimide. By proper selection of stiffener plate adhesive, the plate can easily be removed by placing the assembly on a hot plate at about 150°C. The 20Kg process qualification test specified in MIL-STD-1772 can be performed on mechanical samples.

3.5 Thick-film resistor standardization. Most thick-film hybrid houses use some form of test pattern to control the characteristics of thick-film resistor materials used in fabricating hybrids. David F. Zarnow of NAC has proposed a universal, standardized approach to thick-film resistor fabrication based on extensive investigation and testing both within NAC and at other hybrid supplier facilities. This proposed standard offers the following cost effective advantages:

- o Facilitates the design of thick-film resistors directly from the circuit schematic

- o Precludes the costly, lengthly, and labor-intensive preproduction reliance upon numerous prototype and redesign cycles

- o Only three parameters are required to comprehesively characterize a thick-film resistor system

- o Second sourcing of materials is readily accomplished

- o Reduced costs and better lot to lot consistency through standardization.

3.6 Polymer adhesives and coatings. It has been established that polymeric materials produced in different locations or at different times may exhibit slightly different chemical compositions and physical properties. Methods presently used in the hybrid industry such as infrared spectrum and thermogravametric analysis do not protect against these subtle differences that could cause time-dependant field failures. GPC-elution gradient chromatograms should be run on each lot of polymeric material, i.e., adhesive, coating and particle getters used in hybrid microelectronics fabrication.

MIL-A-TBD on polymeric adhesives is being finalized and will define the minimum testing required to qualify such adhesives for use in military hybrids. It contains a two-part qualification procedure. Part 1 is to be accomplished by the adhesive supplier and is designed to assure the adhesive user that, within certain limits, the material will have lot-to-lot consistency. Part 2 is

performed by the user to assure that the material supplied to him is properly used and controlled.

The design guidelines for hybrid microcircuits, MIL-STD-TBD, sets forth some prohibitions on the use of polymer adhesives. The major restriction is the use of conductive adhesives for primary electrical connections. There is a long term failure mechanism that results in increased electrical resistance at the bond interface. In field use, this mechanism can take several years to develop. To date, no proven theory has been set forth to explain the physics of this mechanism.

3.7 Cleaning. The subject of cleaning hybrids microcircuits is probably the one requiring the most attention. Very thin layers of contamination can result in long term reliability problems. Some of these problems that have been documented are:

- Low activation energy wirebonding failures
- Metal migration
  - Gold
  - Silver
- Soft semiconductor junctions
- "Disappearing" metal

The area of surface chemistry related to hybrid microcircuits should receive considerable attention when considering Research and Development (R&D) projects. Recent studies have indicated great promise in cleaning hybrid microcircuits using plasma technology. The value of plasma cleaning prior to wirebonding has been established by several hybrid manufacturers. Studies have shown that the bonding window for a particular bonder is in-

creased substantially by using plasma techniques. For example, for a plasma cleaned device, the stage temperatures of thermosonic wirebonders are about 20°C lower for the temperature at which bonds just start to stick. This allows for a considerable improvement in the margins between the optimum bond and a defective bond. Plasma cleaning prior to wirebonding helps for monometallic as well as bimetallic bonds.

Evidence has been gathered to indicate more benefits from plasma cleaning. In late 1977, several lots of parts failed the 300°C, 4 hour, wirebond testing and were found to exhibit a failure mechanism with an activation energy of 0.4 rather than the classic 1 ev for the gold aluminum interface. This was traced to organic residue in the bonding pad area (either on the IC's as supplied by the chip vendor or organic residue from epoxy curing or a combination of both). An intensive program was started to use plasma cleaning to remove organics prior to wirebonding. By August 1978 the procedure was instituted in the production line. Since the institution of plasma cleaning, no lots have failed the 300°C bake test. Also, to-date there has been no failure of a semiconductor device on a hybrid that has been plasma cleaned.

The following shows the data from nearly 6000 hybrid microcircuits that have been out in the field for up to 3 years after plasma cleaning:

11 Hybrid Types - 5938 parts

36 months in the field
9,699,698 hybrid operating hours
No semiconductor failures to-date

Linear IC's	37,711,776 hours	= 0.027
Digital IC's	65,250,794 hours	= 0.015
Transistors	75,233,020 hours	= 0.013
Diodes	39,980,520 hours	= 0.025

The wire bonding phase using plasma cleaning has been well documented, but there are still a few minor questions to be answered. These are:

- How long should a part remain in the plasma equipment after it has been cleaned to assure the best product? Quick removal and wire bonding would take advantage of a highly active surface to enhance the wire bonding procedure. However, quick removal will also pick-up more surface moisture which could lead to other problems such as temporary threshold shifts on MOS devices.

- Are wire bond strengths improved to a point where some of the older coatings would not lift the bonds? Some of the thicker types of coatings (such as silicones) formed fillets around the wirebonds. These fillets caused stresses during themal cycling that lifted some wirebonds. Wirebonds removed after plasma cleaning do not separate at the bond pads but typically lift silicon from the semiconductor devices. Therefore, it is possible that the bonds that lifted during thermal cycling using the older, thicker coatings were in fact, poor bonds. With the stronger bonds resulting from plasma cleaning it might be possible to use some of the older, thicker coatings.

The main questions that need to be answered in regard to plasma cleaning for improved wirebonding has to do with secondary processing control problems rather than the major controls that have been well developed and have demonstrated good field reliability. The effect on certain semiconductor devices such as CMOS and high frequency transistors must be better documented. Several different gasses should be evaluated to see if they would show any measurable effects. It has already been reported that hydrogen in a plasma will cause shifts in CMOS threshold voltage which

have to be annealed out. Other gasses may have similar or new effects which have to be documented. Another variable that must be investigated is how long the plasma cleaned surface remains activated. Various methods could be used. One would be to have a moisture monitor on the test hybrid and measure the amount of moisture picked up by the sensor as a function of such things as the time the hybrid remains in the vacuum environment after the plasma has been turned off and before it is brought out into a humidity (both high and low) controlled atmosphere. Another method would be to measure weight gain under similar test conditions.

Care must be taken in setting up plasma processes to assure that secondary problems, such as sputtering gold, are not introduced products. For the removal of thin layers of contaminants (either organic or inorganic), argon gas (probably in-conjunction with available traces of oxygen) has proven effective. A study should be made on the actual mechanisms present in such a cleaning operation.

Plasma processing could be effectively used at several stages of hybrid microcircuit construction. These stages would include:

- Substrate (either polymeric or eutectic) attachment
- Element (either polymeric or eutectic) attachment
- Wirebonding
- Just prior to sealing as an integral part of the sealer

3.8 Internal moisture content. Several recent studies have indicated that some items concerning moisture related problems need further investigation. The study presented in the following paragraphs reports on some observations that were made as a result of a failure analysis on complex hybrid microcircuits. It suggests that failure modes are different for various internal moisture level contents. In a range above 17,000 ppm, semiconductors failed. From about 6000 ppm to 17,000 ppm, nichrome resistors failed, and below 1000 ppm of moisture, no failures occurred. Probably the most significant result of the observations is that, if the moisture content of the parts that had semiconductor failures had not been measured, the failures would never have been classified as moisture related.

As a result of an investigation of failures in some complex hybrid microcircuits, some interesting observations were made concerning moisture related failures. The investigation started as a result of several hybrids that had failed on the first operational cold cycle at board testing level. These parts were found to have the classic "disappearing nichrome resistor" problem. Many more of these hybrids failed and an intensive investigation was started to determine the cause of the failures.

A total of 25 hybrid microcircuits were selected for the investigation. Sixteen of these had failed during system test and nine were parts from the same data code series that had successfully passed all systems tests. All 25 parts were tested for internal water vapor content in accordance with Test Method 1018 of MIL-STD-883. The parts were then delidded and checked both visually and electrically. The electrical testing showed no changes in the previous status, i.e., 16 failures and nine good parts. As expected, the nine good parts showed no visual abnormalities.

Surprisingly, eight of the 16 failures also showed no visual abnormalities. The remaining eight parts all had considerable damage to one or more nichrome resistors. Further testing of the eight failed parts with no visual abnormalities were all confirmed as semiconductor failures. Some of these parts cured themselves shortly (the shortest time was about 48 hours) after they were opened. The remaining parts that had semiconductor failures were restored to working condition during high temperature reverse bias tesing. Some but not all the semiconductor failures could be reinduced when the parts were placed in a humidity chamber.

A review of the part histories of the 16 failures showed that the eight parts that had nichrome resistor damage failed on the first powered cold cycle. The other eight failed parts (semiconductor failure) dropped out randomly during sytem testing. Two of these failed prior to the first cold cycle and one did not fail until final system burn-in.

The data from the internal water vapor tests were rank ordered according to moisture content. This data was plotted (see Figure 9) using different symbols for the three different categories of failure mechanisms (no failures, resistor failures, and semiconductor failures). Figure 10 shows the dew point range for internal moisture content that produced nichrome resistor failures.

The major conclusion that can be drawn from this limited investigation is that unless internal moisture level measurements are made a part of the failure analysis, semiconductor failures will not be properly reported as moisture problems. Other observations that could be suggested by the investigation are:

- If enough moisture is present in the hybrid, then the necessary voltage drop to cause nichrome disappearance may not be present.

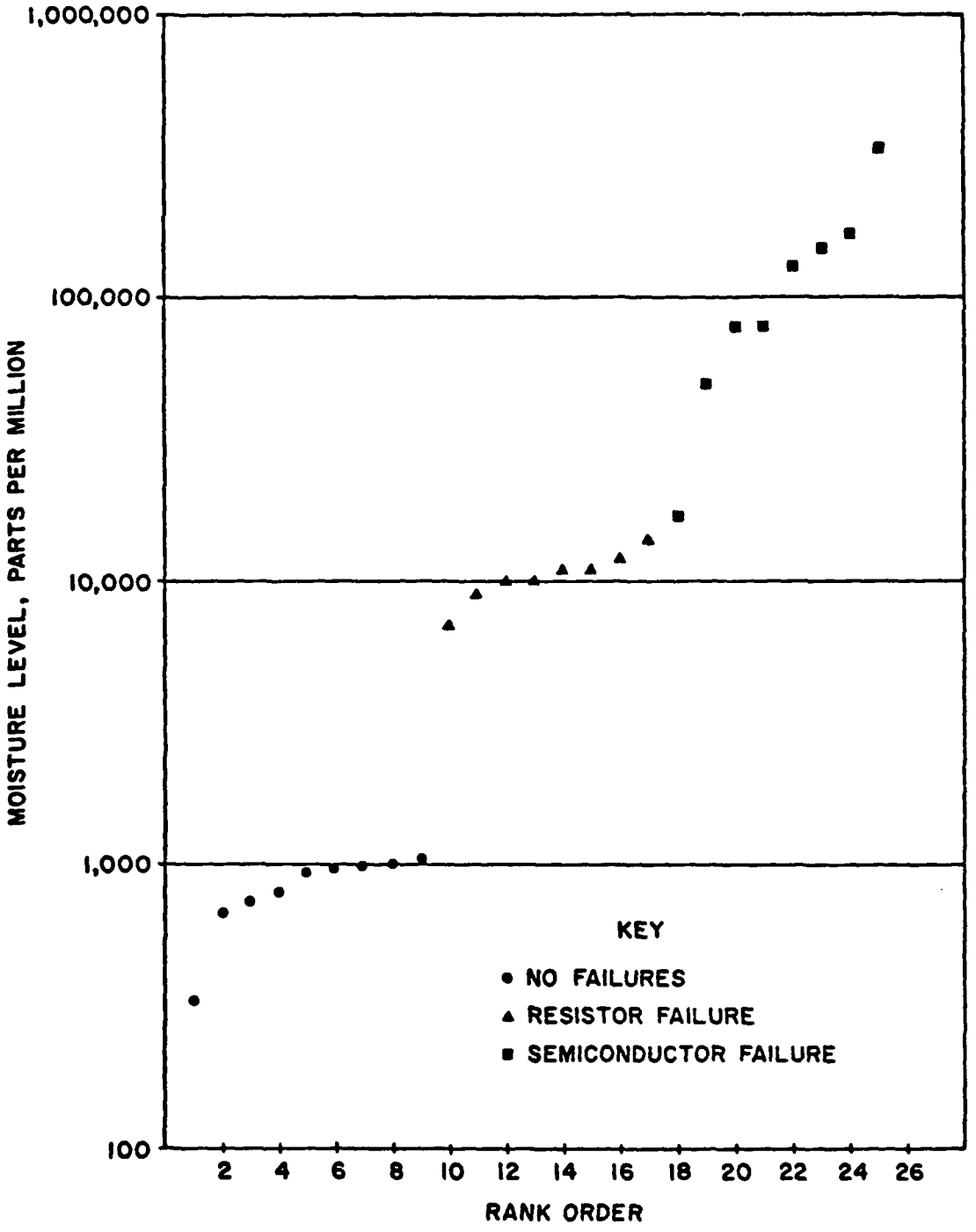

FIGURE 9. FAILURE MECHANISM VS MOISTURE CONTENT

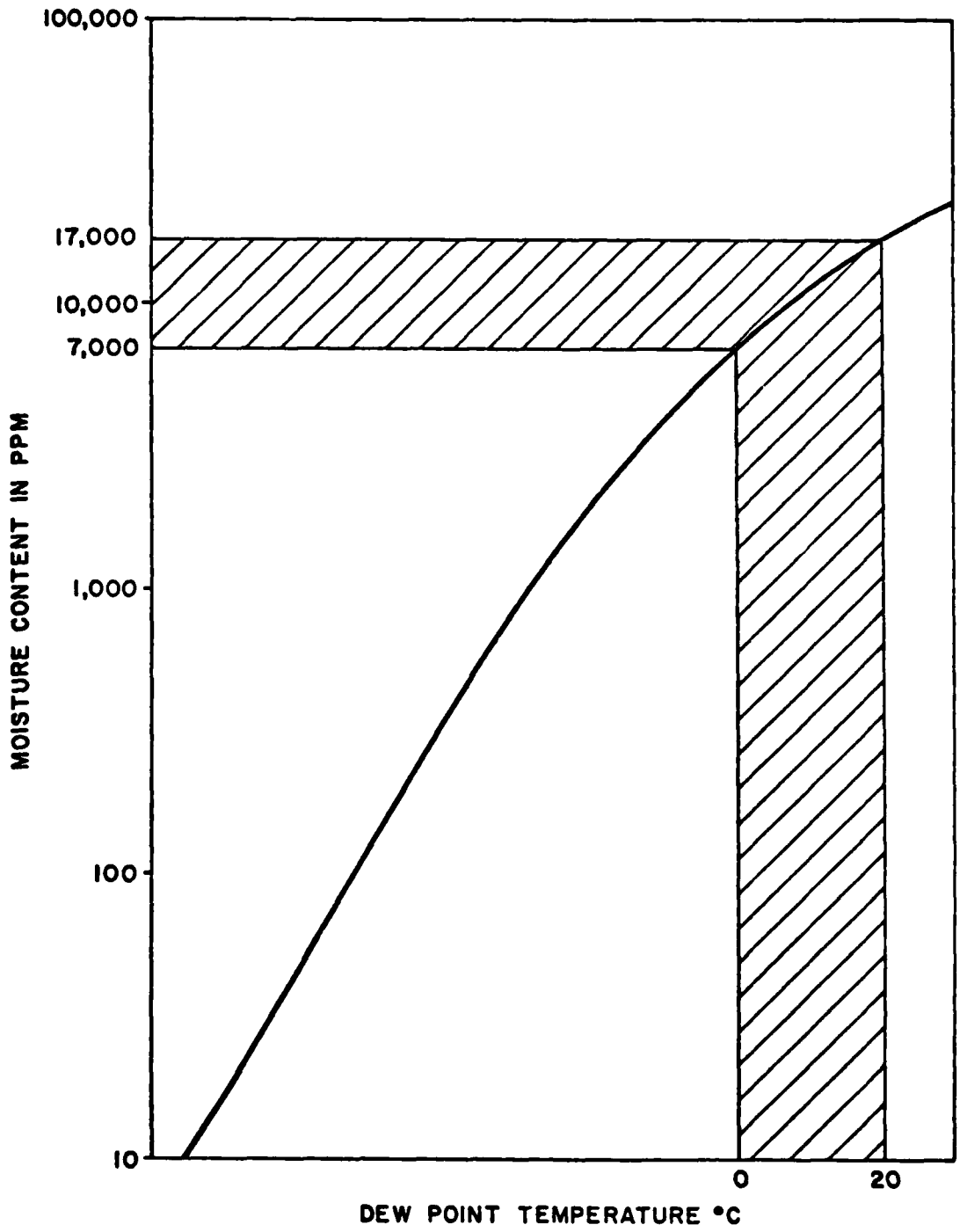

FIGURE 10. DEW POINT RANGE FOR FAILED RESISTORS

- o If the moisture level is below the room temperature dew point, then the effect of the semiconductor failure mechanism will be greatly reduced during room temperature storage.

- o Controlled tests should be run to determine the physics involved in semiconductor failures in the presence of moisture. Particular emphasis should be placed on understanding why some semiconductor failures can be reestablished in the presence of moisture and others cannot.

Care must be taken to assure that the final "bakeout" of moisture before sealing is an integral part of the sealing equipment. It is possible to "bakeout" deep moisture in an off-line oven as long as the transfer time to the sealing oven is reasonably short and the final "bakeout" in the sealing equipment is sufficiently long to remove the surface moisture that has been accumulated during the transfer time. Figure 11 shows a graph that was generated to show how rapidly surface moisture is absorbed in room atmosphere.

The graph shown in Figure 11 shows very clearly that even a short exposure to room ambient (less than 2 minutes) can easily result in unacceptable levels of moisture in the package. Eutectic attach is considerably better than epoxy but, if contamination levels in a hybrid were large, experience has shown that even the 3000 ppm could cause problems. Eutectically attached parts that were vacuum baked in an oven directly attached to a sealer in a moisture controlled(25-50 ppm of water) enclosure routinely had moisture levels at limit of the test equipment, i.e., between 100 and 200 ppm of water when tested in accordance with Test Method 1018 of MIL-STD-883.

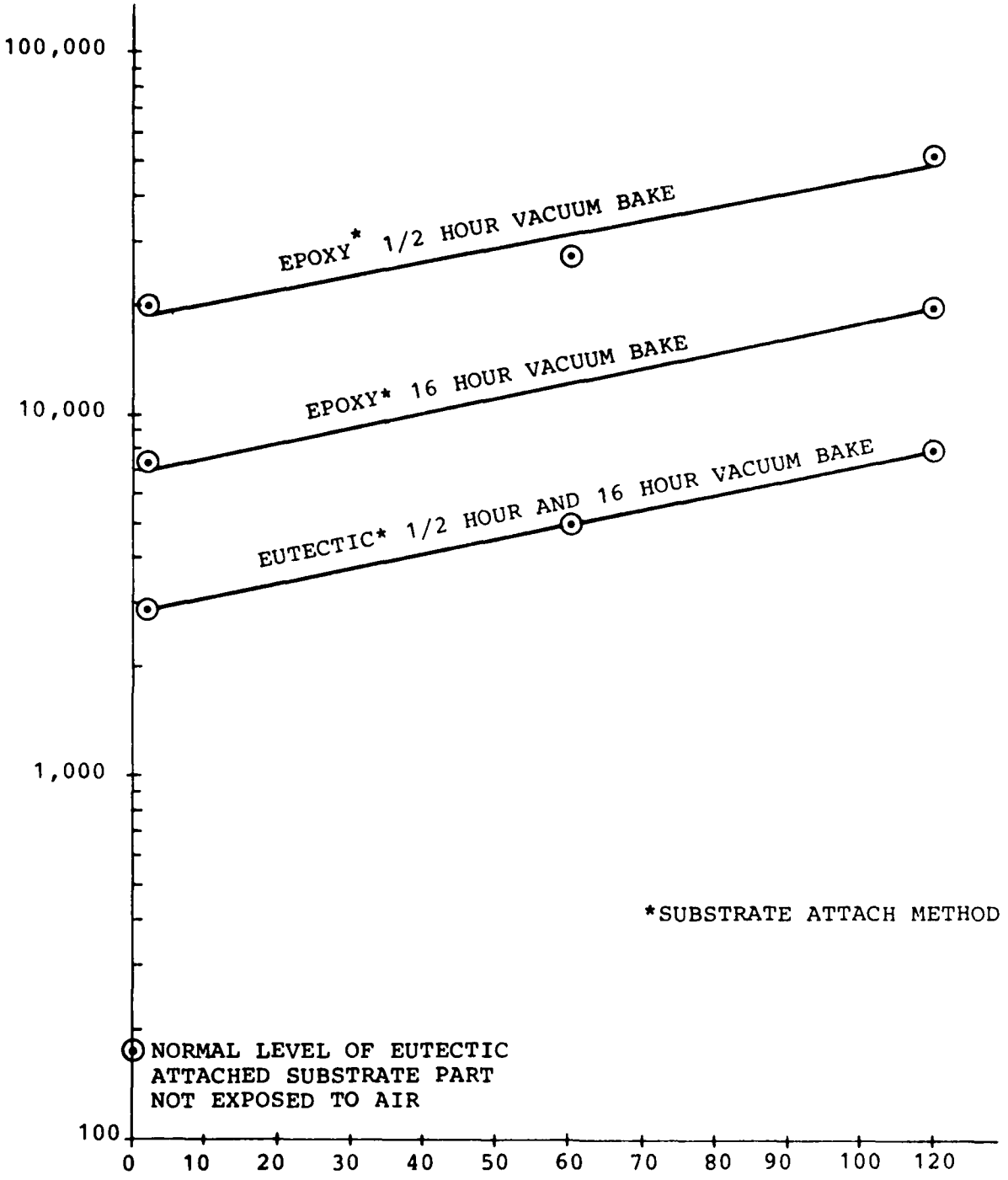

FIGURE 11. THE EFFECT OF PRE-SEAL EXPOSURE TO ATMOSPHERIC CONDITIONS ON HYBRID MOISTURE CONTENT

3.9 Electrostatic discharge. The handling of hybrid microcircuits must consider damage that could be caused by ESD (electrostatic discharge). This concern must be maintained from incoming inspection of the individual elements through field use of the hybrid microcircuits.

Items that are commonly used in hybrid microcircuits that are susceptible to ESD are:

- MOS structures
- Semiconductor junctions
- Metalization stripes
    - Open metalization
    - Short Circuit through adjacent dielectric
    - Short circuit to adjacent conductor
- Resistors
    - Thick film
    - Thin Film
- Piezoelectric crystals

The literature contains a great deal of information of the care and handling of ESD sensitive devices. Generally work stations should be protected by use of:

- Conductive table tops
- Personnel grounding devices such as wrist straps
- Protective floors

- Protective stools
- Air ionizers
- Conductive or antistatic protection or handling containers

The entire ESD problem is one of probability and statistics. There exists a distribution of voltages in a particular area that is available to ESD sensitive devices. There also exists a distribution of threshold voltages that will degrade or destroy items in that area. The problem is to see that the high end of the available voltage distribution is well below the low end of the threshold voltage of the most ESD sensitive device.

The current military documents covering electrostatic discharge are as follows.

- MIL-STD-883, Test method 3015 - "Electrostatic discharge sensitivity classification".
- DoD-STD-1686 - "Electrostatic discharge control program for protection of electrical and electronic parts, assemblies and equipment (excluding electrically initiated explosive devices)".
- DoD-HDBK-263 - "Electrostatic discharge control handbook for protection of electrical and electronic parts assemblies and equipment (excluding electrically initiated explosive devices)".

3.10 Lid deflection. Present requirements for clearance between the lid of a hybrid microcircuit and the highest internal element or interconnecting wire is not well defined. This allows for the possiblity of short circuits between an internal item and the case. The problem is one involving many variables such as:

- o Location of highest item
- o Size of the lid
- o Thickness of the lid
- o Environmental conditions
- o Wall thickness of the case
- o Case and lid material
- o Number of delid and reseal cycles

Because of this, it is recommended that a lid deflection test described in the following subparagraph be run during prototype qualification on a hybrid that has been delidded and resealed one more time than the maximum allowed for that device.

3.10.1 Lid deflection test. Hybrids with external package dimensions exceeding 5/8 of an inch on two edges shall be subjected to the lid deflection test. All leads not attached electrically to case ground shall be connected in parallel. A sensitive ohmmeter shall be connected between the leads connected in parallel and the case while being subjected to a force of 3 pounds applied to the top of the lid. The force shall be applied vertically over an area of 1/16 of a square inch at the center of the lid. Any evidence of internal items shorting to the case shall require corrective action.

3.11 Glass-to-metal-seals. Based on the experience of several hybrid manufacturers, several users and the experience of the National Bureau of Standards, the following conclusions have been obtained:

a. Thermal Shock tests appear to be effective on a lot rejection bases.

1. If a lot of screened packages passes the first thermal shock test on a 100% basis, then those parts will not exhibit glass-to-metal seal problems during processing or use even if the parts are abused and the glass is grossly cracked.

2. If the parts do not pass the first shock test on a 100% basis, then the lot will exhibit seal problems during processing and use, even if several shock tests are used to screen the lot.

b. Visual examination of glass beads is counterproductive.

c. All glass-to-metal seal problems investigated to date show leaks at the glass-to-metal interface and not through the glass.

One of the problems associated with the present method of He/Mass spectrometer systems is that moisture and helium enter the package by different mechanisms. Some parts that fail the helium test may not leak moisture and conversely, many parts that pass the helium test will allow moisture into the package.

High temperature dye penetrants have been shown to be effective in both screening and performing failure analyses on packages using glass-to-metal seals.

Visual examination has been demonstrated by controlled experiment to be counterproductive. The tendency of inspectors is to either pass everything or fail everything. Samples containing both good (checked by He/Mass spectrometer and high temperature dye penetrant) and bad seals were subject to visual screening by six observers. There was no correlation between the visual and actual rejects.

3.12 Visual inspection. Personnel responsible for visual inspection accept/reject decisions on hybrid microcircuits should be well trained and be aware of the physical reasons for the criteria contained in Test Methods 2008,2010,2013,2014 and 2017 of MIL-STD-883, and 2072 and 2073 of MIL-STD-750.

Visual inspectors should be trained to follow a routine series of steps so that all the details will be observed on each inspection. One such routine is listed as follows:

a. Lowest magnification (10X) sweep of the entire hybrid looking for gross defects and large loose particles. Particular attention should be paid to the well area between the substrate and the package for substrate attachment and loose particles.

b. Using slightly higher magnification, survey the substrate for any weld tails or foreign material. The part should be tilted or side lighting used to accentuate these potential deficiencies.

c. Using the upper end of the low magnification (about 60X), carry out the remainder of the low magnification inspection.

    1. Substrate defects - Make sure that cracked substrates are considered. Polarized lights are beneficial for this inspection. It is also beneficial to check for metal smearing and migration.

2. Passive elements - Check passive element components for both element defects and attachment quality.

3. Active elements - Check active elements for attachment quality.

4. Wirebonds - Check for wirebonding compliance with the visual requirements.

d. Perform high magnification active element inspection.

3.13 Hidden hybrids. Several devices, such as switches, relays and timers, were at one time considered electromechanical. These devices as well as items like oscillators, have with the advent of semiconductor microtechnology, become hybrid microcircuits. As such, they must meet MIL-STD-883 and MIL-M-38510 requirements in order to be used in Government programs.

It is recommended that all devices such as switches, relays, timers and oscillators be subjected to a Destructive Physical Analysis (DPA) before they are approved for use on contracts requiring conformance to MIL-STD-883 and MIL-M-38510. If the DPA determines that the device is, in fact, a hybrid, then some sort of satisfactory documentation such as a Specification Control Drawing (SCD) containing the applicable requirements of MIL-STD-883 and MIL-M-38510 must be generated. The SCD shall, as a minimum, impose the requirements of Test Methods 2017 and 5008 of MIL-STD-883 and the requirements of Appendix G of MIL-M-38510.

Also, a review of military specifications concerning these "hidden hybrids" should be made and a note added calling for MIL-STD-883 and MIL-M-38510 requirements if these devices fit the definition of a hybrid. In particular, any devices purchased in accordance with the following military specifications should be carefully reviewed to determine if it should be classified as hybrids.

MIL-O-55310	Oscillator, Crystal
MIL-R-39016	Relay, Electromagnetic
MIL-R-28750	Relay, Solid State
MIL-M-7793	Meter, Time Totalizing

3.14 Percent defective allowable. The Percent Defective Allowable (PDA) concept originated with the semiconductor industry and was not based on a rigorous statistical approach. It was used as a sampling plan, based on normal process yield, to determine if a particular lot required 100% screening. PDA was devised to allow simple testing rather than using cumbersome sampling plans such as those based on the Weibull approach.

The concept was then misapplied to custom hybrids on a 100% basis. This has caused a great deal of problems since the PDA concept does not apply to small lots with unknown lot-to-lot yields.

A better concept for hybrids would be one of pattern failures. More drift failures should be allowed than catastrophic failures. It is recommended that this concept be used in Test Method 5008 of MIL-STD-883 and Appendix G of MIL-M-38510 in place of the present PDA requirements. Table 1 lists the recommended changes from PDA to pattern failures for the specific paragraphs of Test Method 5008 of MIL-STD-883.

TABLE 1. RECOMMENDED CHANGES FROM PDA TO PATTERN FAILURE, TEST METHOD 5008 OF MIL-STD-883

3.4.9.a Preburn-in electrical testing is optional except when delta limit measurements are required. However, devices may be tested to remove pattern failures.

3.4.10.c A maximum number of pattern failures (failures of the same part type when the failures are caused by the same basic failure mechanism) shall apply as specified in the procurement document. If not otherwise specified, the maximum allowable pattern failures shall be as follows:

LOT SIZE	CATASTROPHIC	DRIFT
20 or less	2	3
greater than 20	3	5

Accountability shall include burn-in through final electrical test.

3.4.10.d When the number of pattern failures exceeds the specified limits, the inspection lot shall be rejected. At the manufacturers option, the rejected lot may be resubmitted to burn-in one time provided:

(1) The cause of failure has been evaluated and determined.

(2) Appropriate and effective corrective action has been completed to reject all devices affected by the failure cause.

(3) Appropriate preventative action has been initiated.

TABLE I. (CONTINUED)

4.0.d Delta parameter measurements or provisions for pattern failure limits including accountable parameters, test conditions, and procedures for traceability, where applicable.

3.15 Failure analysis consideration. As hybrid manufacturers become more experienced and have better controls on their processes and precedures, failure mechanisms become more subtle. The detection of these mechanisms require more sophisticated equipment and better trained analysts. In order to improve hybrid reliability and cost effectiveness, it is imperative that users work closely with hybrid suppliers on field failure problems. This is particularly true of time dependant failures that the hybrid manufacturers would have little or no awareness of without cooperation from the user.

The physics related to many of the current problems found in hybrids are discussed in the literature and elsewhere in this report. Failure analysts should be aware of the latest methods of analyses in at least the following areas:

- Internal Moisture Content
- Hermeticity Testing
- Thin Layer Surface Contamination
- Loose Particle Detection and Recovery
- Polymeric Adhesives

When selecting a supplier for military grade hybrids, it is imperative that a potential candidate be carefully reviewed to determine the ability to perform sophisticated analyses on their product. The total analysis capability need not reside within the hybrid manufacturer facility, but an awareness of the problems and a knowledge of where and how to proceed with a critical analysis must be demonstrated.

On the other hand, the hybrid users must also have the ability to detect, analyze and correctly categorize a failure. Users must also be able to report back to the hybrid supplier the long term changes in reliability (both positive and negative) resulting from changes in processes, procedures and materials.

3.16 Particle getter. The sealing of hybrid microcircuits that will meet the Particle Impact Noise Detection (PIND) Test in accordance with Test Method 2002 of MIL-STD-883 has created the need for a new method of immobilizing particles. A material called a "particle getter" has successfully been developed by several hybrid manufacturers. This material is polymeric and is deposited on the lid of the hybrid package. The primary concerns in qualifying a particle getter are:

- Permanent and efficient entrapment of loose particles over a wide range of environmental stresses.
- Stability under all processing and use conditions.
- No degradation of the hybrid performance or repairability by the effects of outgassing of the getter material.

In order to qualify the particle getter process, a comprehensive test program must be completed. The test program must consider, as a minimum, the following items:

- Possible corrosive outgassing during cure.
- Affect of outgassing on thin film metalization.
- Affect of outgassing on wirebonding (both initially and during repair or rework cycles).

- Affect of outgassing on surface sensitive semiconductor devices.

- Moisture levels after 1000 hour bake at 150°C.

- The ability of the getter material to trap and hold typical loose particles over the entire temperature range and throughout the life of the hybrid.

- The ability of the getter material to hold typical loose particles when subjected to high level mechanical shock.

- Develop the documentation to assure the process that was qualified will stay under control.

- Develop in process screening to assure that the process remains in control.

The approval for the use of particle gettering does not negate the requirement for the performance and passing of PIND testing.

4. SUMMARY OF TODAY'S TECHNOLOGY AND FUTURE TRENDS

Today's hybrid microcircuit technology is capable of building compact, reliable products. Techniques have been developed to greatly reduce or eliminate problems that recently plagued the industry. These include:

- Control of internal moisture
- Development of standard polymer testing
- Control of detrimental intermetallic formation at wirebond interfaces

Now the major technical problems emerging are those having to do with ultra thin film surface chemistry and wedge bonding to thick film gold. Plasma cleaning seems to hold the key to the solution of the surface chemistry problems. While automatic wirebonding will hopefully mature to the point of solving the wedge bond problem.

Cost is still the major disadvantage of hybrid microcircuits. Again, a better understanding of surface chemistry and the improvement in automatic wirebonding (including pattern recognition) will aid in the yield and thus reduce the cost.

5. CONCLUSIONS

During the two years of this contract, the hybrid industry has matured considerably. This is, in large part, due to the excellent spirit of cooperation that has existed between hybrid suppliers, systems suppliers and government agencies. By hard work and compromising by all of the interested parties, the present military specifications have resulted in a cost effective set of quality assurance documents for hybrid microcircuits.

The basic philosophy behind the documents generated as part of the contract was to develop a cost effective approach to controlling military hybrids. The documents covered both B and S level products. The complete set of documentation should allow for better communications between hybrid suppliers and hybrid users. The attempt was made to achieve this goal by standardization of the minimum amount of testing and controls necessary to assure reliable product.

Both hybrid users and suppliers should become familiar with the total package of documents since they were designed to be mutually supportive. If either hybrid users or suppliers find that these documents are lacking in some areas, too restrictive in other areas, not cost effective or are ambiguous, they should forward constructive comments and suggestions to:

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A review of the final package has revealed several areas where comments and suggestions are solicited. These are as follows:

a. Die Shear - The present curve in test method of MIL-STD-883 does not cover small area die. The curve

cuts off at die areas above what is normally found in hybrids leaving an area of ambiguity. The suggestion is put forth here to simply extend the curves in a linear fashion through the 0 point. The rationale for this is that, on the one hand strengths should be higher due to the "edge effect of the die adhesive", but on the other hand alignment of the die shear tool is more difficult causing die shear strengths to be too low.

b. X-Ray - The criteria for X-Ray needs to be revised to be more cost effective for hybrids. Many of the requirements are ambiguous and experience has shown that in a number of cases where further testing was done to follow up X-Ray rejects, results showed that good parts were being rejected. This has been particularly true in the cases where PIND testing or centrifuge was used to verify the results.

c. Hidden Hybrids - Hybrids disguised as items such as oscillators and relays have escaped the testing of MIL-STD-883, Test Method 5008. This is a difficult area to control. It is suggested that the military consider putting a statement in their procurement documents that would call for a review of components specifically designed to uncover "hidden hybrids". Once located, the component procurement specifications should require the necessary hybrid documentation to assure reliable product.

d. Chip Testing - The JEDEC JC-13.5 committee is presently developing the documentation necessary for testing chips to be used in hybrids. This specification is nearing its final form. When this is completed, it should be reviewed for inclusion into the present set of hybrid documentation.

e. Residual Gas Analysis - This is an area where more data and testing are required. At present, only moisture levels are specified. There has been some data to indicate that the presence of ammonia and ethanol could be detrimental to the reliability of hybrids. The effects of other materials should also be considered.

Appendix A

Sample

GENERAL SPECIFICATION

FOR

HYBRID MICROCIRCUITS

Y125A18.0

(This sheet reserved for Revision Record information)

GENERAL SPECIFICATION

FOR

HYBRID MICROCIRCUITS

1. SCOPE

1.1 General. This specification covers the general requirements for hybrid microcircuits used in airborne and missile programs where reliable performance is required. Circuits supplied to this specification shall comply with all requirements of MIL-M-38510, MIL-STD 883 and the detail design, construction, mechanical, electrical and environmental requirements specified here. Specific requirements for a particular type of hybrid microcircuit are listed in the applicable detail drawing.

1.2 Qualifying Activity. For purposes of compliance to MIL-M-38510, and for this specification, the Halmatic Division of the Bendel Company shall be deemed the qualifying activity; all documents required by MIL-M-38510 shall be submitted to or be made available to Halmatic Division as applicable.

1.3 Manufacturer's Qualification. The manufacturer shall submit test data to demonstrate that the manufactured microcircuit is in compliance with all requirements of this specification and the detail specification.

1.4 Approved Sources. When the manufacturer's qualification is complete, to the satisfaction of Halmatic Division, the manufacturer shall be listed on the detail drawing as an approved and qualified source of supply for the microcircuit.

1.5 Manufacturing Changes. After qualification approval by Halmatic Division, the manufacturer shall comply with MIL-M-38510 with regard to change in design, material or processes. The manufacturer shall not implement any change prior to receipt of written authorization from Halmatic Division procurement activity. Halmatic Division may specify special testing as a result of any change in order that a manufacturer may retain qualification status. Similarly, following periods of procurement inactivity the manufacturer shall notify Halmatic Division of any change that has been introduced since the previous procurement that will affect microcircuits supplied to the new procurement.

1.6 Responsibility for Tests and Inspection. Unless otherwise specified in the purchase order, the manufacturer is responsible for the performance of all tests and inspections described in this specification.

Halmatic Division reserves the right to witness or to perform any tests and inspections described in this specification or in the detail drawing, to re-inspect for any requirement, to audit the manufacturer's test data relevant to the performance of the tests and inspections, and to take the following actions:

A. Reject any individual microcircuit that does not meet all specified requirements.

B. Reject any lot that does not meet LTPD's specified in the detail drawing or in referenced documents when re-inspected at Halmatic Division.

Re-inspection or testing shall be performed within 60 days of receipt of completed microcircuits by Halmatic Division.

1.7 Classification of Microcircuits.

1.7.1 Group I Microcircuits. Microcircuits which are modifications of a manufacturer's 'standard' item with additional requirements imposed by Halmatic Division.

1.7.2 Group II Microcircuits. Microcircuits designed to Halmatic Division specifications. Such circuits do not correspond to a manufacturer's standard item. The design and construction requirements are applicable to microcircuit designs provided by Halmatic Division.

Acceptance criteria for features of a manufacturer's design not adequately covered by MIL-M-38510 shall be clarified by supplementary written agreements between Halmatic Division and the manufacturer.

Final acceptance of a design layout is subject to approval by Halmatic Division.

1.8 Definitions. Terms and definitions are in accordance with MIL-M-38510 with particular terms noted here.

1.8.1 Production Lot or Inspection Lot. All microcircuits supplied to the same set of specifications and control documents, produced in a continuous production cycle, using the same production techniques, materials and processes for a period not to exceed six (6) months shall be considered the same production lot.

1.8.2 Defective Microcircuit. A microcircuit which malfunctions or does not meet the acceptance criteria of this specification or of the detail drawing is a defective microcircuit. Defective microcircuits shall be removed as soon as they are identified and shall not continue in the test sequence. The quantity of defectives removed at each point shall be noted on the lot history or traveler record.

1.8.3 Lot Failure. A lot, whether at screening or inspection, in which the number of defective microcircuits exceeds the allowed number of defectives is a lot failure.

1.8.4 Percent Defective Allowable (PDA). The PDA is specified as 10 percent based on defective microcircuits at electrical testing after burn-in. If interim electrical parameter tests are performed prior to burn-in, defective microcircuits identified at per-burn-in may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, then all defective microcircuits not identified prior to burn-in shall be included in the PDA. The verified defective microcircuits after burn-in divided by the total number of microcircuits submitted for burn-in in that lot shall be used to determine the percent defective for the lot, and the lot shall be accepted or rejected based on the PDA.

1.8.5 Traceability. Traceability shall be in accordance with the requirements of MIL-M-38510 Appendix G.

1.8.6 Rework. Rework is an operation performed on a nonconforming microcircuit so that it complies with the engineering drawing and referenced specifications. The constructional aspect of rework is accomplished by using the same processes as were used in the original construction of the assembly.

Examples of rework:

A. Correction of wirebonds: Removal of defective wirebonds (mechanically unacceptable or electrically misconnected) and placement of new wirebonds

B. Components: Removal of defective component and replacement by a new component reattached by the same method.

C. Trimming of passive components

D. Relidding of package

1.8.7 Repair. Repair is an operation performed on a nonconforming microcircuit to make it functionally usable; the repaired microcircuit does not completely conform to the engineering drawing and its referenced specifications. In the constructional aspect of repair, it is not possible to use the same processes as were used in the original construction of the microcircuit.

Examples of repair:

A. Use of an organically attached molytab when replacing a semiconductor chip component where damage to the substrate metallization precludes rework

B. Replacement of a defective deposited resistor by a chip resistor

C. Change from a specified material to material with a lower temperature characteristic (organic or eutectic) to prevent degradation of adjacent devices which may be temperature sensitive.

D. Replacement of a damaged printed conductor by a wire. Note: Wire bonds cannot be used to compensate for problems in metallization on semiconductor chips or on other components in chip form.

2. APPLICABLE DOCUMENTS

2.1 The following documents, of latest issue in effect at the time of request for quotation, form a part of this specification to the extent specified.

SPECIFICATIONS

Military

MIL-S-19500	General Specification for Semiconductor Devices
MIL-M-38510	General Specification for Microcircuits

STANDARDS

Federal

FED-STD 209	Clean Room and Work Station Requirements, Controlled Environments

Military

MIL-STD 883	Test Methods and Procedures for Microelectronics
DOD-STD 1686	Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies and Equipment
MIL-STD 1772	Product Assurance Provisions for Custom Hybrid Microcircuits

2.2 In the event of conflict between requirements of documents, the order of precedence is:

A. Purchase order and ancillary documents

B. Halmatic Division documents
   1. Applicable microcircuit drawing (detail specification or drawing)
   2. This specification

C. Military documents referenced in 2.1

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified here and in the detail drawing. Only microcircuits which are inspected for and meet all requirements shall be delivered.

3.2 Documentation.

3.2.1 Group I - Approval. The manufacturer shall submit the following documents for written approval and shall make no change prior to written agreement by Halmatic Division.

A. Burn-in procedure

B. Inspection procedures for organic materials

C. Workmanship specifications covering all levels of assembly and inspection

D. Rework procedures covering rework performed at all levels of assembly or inspection

3.2.2 Group I - Informational. The manufacturer shall submit the following documents for information only.

A. Microcircuit assembly layout drawing plus supporting identification of all materials not identified on the drawing

B. Parts list: internal parts through finished, packaged assembly

C. Process flow charts showing all steps from receipt of materials through shipment of completed microcircuits including microcircuits returned from Halmatic Division, identifying all controlling documents

D. Acceptance test procedure

E. Circuit element specifications: procurement or performance specifications showing approved suppliers

F. List of suppliers of each semiconductor device and microcircuit chip

3.2.3 Group II - Approval. The manufacturer shall submit the following documents for written approval and shall make no change prior to written agreement by Halmatic Division.

A. Microcircuit schematic

B. Microcircuit assembly layout drawing plus supporting identification of all materials not identified on the drawing.

C. Parts list: internal parts through finished, packaged assembly.

D. Attachment materials: identification of materials used for attaching chip components to the substrate, and for attaching the substrate to the case.

E. Thermal analysis for power transistors and criteria for 100 percent verification that these transistors meet the junction temperature requirements of the detail drawing.

F. Analysis for temperature coefficients for resistors and capacitors; 100 percent verification that these components meet the temperature coefficients specified in the components list corresponding to the detail drawing.

G. Process flow charts showing all steps from receipt of materials through shipment of completed microcircuits including microcircuits returned from Halmatic Division, identifying all controlling documents.

H. Acceptance test procedure and associated test set schematic.

I. Burn-in procedure and associated test fixture schematic.

J. Circuit element specifications: procurement or performance specifications showing approved suppliers.

K. List of suppliers of each semiconductor device and microcircuit chip.

L. Inspection procedures for organic materials.

M. Workmanship specifications covering all levels of assembly and inspection.

N. Rework procedures covering rework performed at all levels of assembly or inspection.

3.2.4 Photograph. The manufacturer shall supply the following in place of the die photograph required in MIL-M-38510 design documentation: one 35 mm positive color transparency of the microcircuit conforming to the design documentation requirements of MIL-M-38510. Adequate magnification shall be used such that 75 percent of the area on the 35 mm positive color transparency shows the wirebonded die and includes the edges of the package but not the full length of the external leads.

3.3 Physical and Mechanical Characteristics.

3.3.1 Physical Dimensions. The physical dimensions shall be in accordance with the outline dimensions in the detail drawing.

3.3.2 Package Construction.

A. Materials. The package shall be primarily a metal package with glass or ceramic used only for lead isolation. Glass frit packages shall not be used. Package materials shall be in accordance with MIL-M-38510 with the following particulars:

1. Case material and lid may be kovar, nickel, or steel finished with gold plate or other non-corrosive finish in accordance with MIL-M-38510.

2. Lead material shall be kovar and lead finish shall be in accordance with MIL-M-38510.

B. Package lead frame shall conform to the number of pins required; pins shall not be clipped off.

C. Lead Emergence. The glass meniscus (glass protrusion from case outline along the lead length) formed at lead emergence shall not exceed 15 mils. The manufacturer shall provide controls for the lid or cover sealing operation such that any solder or similar sealing material does not flow onto or vertically overhang the insulator. Where individual lead insulators are employed, the flow shall not reach the periphery of the lead insulator and there shall be visibly unwetted or clean case surface under 4 power magnification still surrounding each insulator after case seal.

3.3.2 (Continued)

D. Case Isolation. All leads, except those leads connected to the case, shall be electrically isolated from the case. Microcircuits shall be capable of meeting 100 megohms minimum between all isolated leads tied together and the case when tested in accordance with Method 1003 of MIL-STD-883, Level D.

E. Lead Condition. All leads shall be intact and aligned in their normal lead plane free of twists, nicks, sharp or unspecified bends (warping or skewing), corrosion or any other condition which would interfere with the assembly or normal application of the circuit.

3.3.3 Appearance. The package shall be free of foreign material such as paint or other adherent deposits, dust, defective plating (peeled, flaked, or blistered), or damaged plating (nicked or scratched), dents, corrosion or any other condition which could interfere with the application of the circuit or substantially degrade its cosmetic appearance.

3.3.4 Solderability. Delivered microcircuits shall be capable of passing the test requirements of Method 2003 of MIL-STD-883, including steam aging. In addition, microcircuits shall be capable of meeting Method 2003 without steam aging for one year after delivery.

3.3.5 Sealing.

A. All circuits supplied under this specification shall be hermetically sealed in packages which are primarily metal packages, backfilled with inert dry gas(es) at one atmosphere pressure. Hybrid microcircuits with test or specification voltage levels exceeding 100 volts shall be backfilled with inert dry nitrogen gas: 99 percent pure, minimum, as measured at the sealing chamber inlet.

B. Packages shall not be sealed using organics. Upon completion of the sealing process, the seal shall be smooth, continuous and uniform in color and appearance. Rework of the package seal by the application of additional sealing material to the external portion of the package is unacceptable. Rework of the package seal shall be in accordance with the rework provisions of MIL-M-38510 unless otherwise approved by Halmatic Division.

3.4 Marking.

3.4.1 General. Marking shall be in accordance with MIL-M-38510 except the following marking shall be omitted from the circuit but shall be retained on the initial container.

A. Country of origin

B. Manufacturer's identification

If a microcircuit package contains beryllium oxide the part shall be marked with the designation "BeO".

3.4.2 Content and Placement. Microcircuits shall be legibly and permanently marked with the following information as shown in this specification.

3.4.2.1 Group I Microcircuits -- Figure 1.

Top of package:
Manufacturer's name or symbol
Manufacturer's unique part number
Date code
Lot number
Serial number
Terminal identification (pin 1 locator)

Bottom of package:
Optional manufacturer information

3.4.2.2 Group II Microcircuits -- Figure 2.

Top of package:
Bendel Halmatic FSCM Number: 77701
Halmatic part number = drawing number + dash number
Date code
Lot number (when required)
Serial number
Terminal identification (pin 1 locator)

Bottom of package:
Optional manufacturer information

3.4.3 Marking Permanence. Markings on the microcircuit shall remain legible and there shall be no evidence of deterioration of body finish or materials when the microcircuits are subjected to the solvent tests of Method 2015 of MIL-STD 883.

3.4.4 Serialization. Each microcircuit shall be marked with a unique serial number. Each production lot shall have a consecutive block of serial numbers assigned to it and the manufacturing facility shall maintain a record system that provides traceability back to the production lot. In addition to the unique serial number, each microcircuit shall be marked on the side or bottom of the package with a unique number (which at the manufacturer's option may be the same as the unique serial number) prior to internal visual inspection. Traceability records shall be retained for at least 2 years.

3.5 Element evaluation.

3.5.1 General. The term 'element' refers to chip components used in the fabrication of hybrid microcircuits; the term includes active devices as well as passive devices.

Each element shall be subjected to sufficient testing to assure its conformance to requirements in its detail specification and to assure its compatability to assembly and manufacturing processes. As a minimum, each element shall be tested for characteristics which cannot be verified after assembly - characteristics which could cause functional failure during assembly and testing and characteristics which could degrade overall reliability of the completed microcircuit.

Element evaluation may be performed either by the element supplier or by the manufacturer of the microcircuit.

3.5.2 Microcircuit Dice and Semiconductor Dice.

3.5.2.1 Definitions. The term 'microcircuit dice' refers to monolithic microcircuits and similar devices constructed as combinations of simple devices on a single silicon chip. The term 'semiconductor dice' refers to discrete semiconductor devices such as diodes and transistors usually formed as one device per chip.

3.5.2.2 Electrical Tests. Each die shall be electrically tested at 25 degrees C in accordance with the parameters, test conditions and limits in its detail specification.

Electrical testing may be done at the wafer level provided all failures are identified and then removed from the lot when the dice are separated from the wafer.

3.5.2.3 Visual Inspection. Each die shall be visually inspected to assure conformance to the applicable requirements of Method 2010 of MIL-STD 883 and with Method 2072 or 2073 of MIL-STD 750 and with the detail specification.

3.5.2.4 Processing Tests. A sufficiently large sample of randomly selected dice shall be used for tests in Subgroups 1 and 2. Each sample shall be assembled into suitable packages by means of the same assembly methods and functional conditions which apply to the element in its intended application.

3.5.2.5 Subgroup 1. The sample size shall be 10 dice per inspection lot. For internal visual inspection, temperature cycling, and final electrical testing, the minimum requirements for microcircuit dice shall include Subgroups 1, 2, 3 and 4 or 7 in Group A of Method 5008 of MIL-STD 883, and the minimum requirements for semiconductor dice shall include Subgroups 2, 3 and 4 in Group A of MIL-S-19500.

3.5.2.6 Subgroup 2. For each wafer lot, a sample of at least 5 dice requiring a minimum of 10 wire bonds shall be selected.

For wire bond strength testing:

A. Each wire bond shall be nondestructively tested.

B. A minimum of ten wires, consisting of chip to package bonds, shall be destructively pull tested. An equal number of bonds shall be tested on each sample die.

C. The die metallization shall be acceptable if no failure occurs. If only one wire bond fails, another sample shall be selected for Subgroup 2 evaluation: 5 dice with a minimum of 10 wire bonds. If the second sample contains no failures, the bonding test results are acceptable. If the second sample contains one or more failures, or if more than one failure occurs in the first sample, the lot shall be rejected.

D. The rejected wafer lot may be resubmitted to Subgroup 2 evaluation if the failure was not due to defective die metallization.

3.5.3 Passive Elements

3.5.3.1 Electrical Tests. Each element shall be electrically tested at 25 degrees C in accordance with the parameters, test conditions, and limits in the detail specification. As a minimum, the following characteristics shall be tested:

A. Resistors: DC Resistance

B. Capacitors:

Ceramic type - Dielectric withstanding voltage, insulation resistance, capacitance, and dissipation factor.

Tantalum type - DC leakage current, capacitance, and dissipation factor.

Metal insulation semiconductor type (MIS) - DC leakage current, capacitance, and dielectric withstanding voltage.

C. Inductors: DC resistance, inductance, and Q.

3.5.3.2 Visual Inspection. A sample of elements, based on LTPD of 10, shall be visually inspected to assure conformance to the applicable requirements of Method 2017 of MIL-STD 883.

3.5.3.3 Processing Tests. A sufficiently large sample of randomly selected elements shall be used. Each sample shall be assembled into suitable packages by means of the same assembly methods and functional conditions which apply to the element in its intended application. The sample shall contain at least 20 wire bonds (an equal number on each element) if the operation is applicable.

3.5.3.3.1 Visual Inspection. Elements shall be visually inspected for evidence of corrosion or damage attributable to assembly and processing operations.

3.5.3.3.2 Wire Bond Tests. Wire bond strength testing applies to elements which are wire bonded during the microcircuit assembly operation. The sample shall include at least 5 elements with a minimum of 10 bond wires.

A. Each wire bond shall be nondestructively tested.

B. A minimum of ten wires, consisting of element to substrate and package bonds, shall be destructively pull tested. An equal number of bonds shall be tested on each sample element.

C. The element metallization shall be acceptable if no failure occurs. If only one wire bond fails, another sample shall be selected from the remaining elements in the evaluation sample, and subjected to tests in B above. If the second sample contains no failures, the bonding test results are acceptable. If the second sample contains one or more failures, or if more than one failure occurs in the first sample, the lot shall be rejected.

D. The element inspection lot may be resubmitted for evaluation if the failure was not due to defective element metallization.

3.6 Internal Design and Construction.

3.6.1 General. This section covers the criteria for design and construction of hybrid microcircuits. The items are not contained in MIL-M-38510. Workmanship is described in another section of this document. Final acceptance of a design layout is subject to approval by Halmatic Division.

3.6.1.1 Organics. The use of epoxies, lacquers, varnishes, coatings, adhesives, greases or other organic or polymeric materials outside or inside the package is subject to prior written approval by Halmatic Division.

3.6.1.2 Conductive Epoxy. Conductive epoxy shall be silver or gold filled. Conductive epoxy is permitted for making primary electrical connections in hybrid microcircuits in the following cases:

A. Attachment of gold plated kovar or molybdenum tab to substrate conductor.

B. Chip capacitors may be mounted using conductive epoxy on the end caps. In addition, large capacitors shall have nonconductive epoxy under the center of the body. (See "Chip Mounting" in this document.)

3.6.1.3 Clearance. Adequate provision shall be made for the physical size and location of components and wirebonds to ensure that there is minimum clearance of 15 mils between any component and the lid, and between any wirebond and the lid.

3.6.1.4 Detail Requirements. Requirements considered good design practice shall be followed. Exceptions require Halmatic Division approval. The supplier must be prepared to justify each deviation on the basis of cost, producibility, performance or reliability improvements and to show that such deviation will not degrade reliability.

3.6.2 Substrate Layout.

3.6.2.1 Definitions.

A. Multilevel is two or more layers of metal used for interconnection that are isolated from each other by intervening insulation material.

B. A stacked substrate is defined as any object larger than 250,000 square mils mounted on another substrate. This includes substrates, resistor arrays, silicon chips, etc..

3.6.2.2 Detail Requirements.

A. Design of the substrate layout shall meet the breakdown voltage limits appropriate to the individual hybrid microcircuit.

B. Substrates shall have 10 mil minimum edge clearance for conductors and other elements.

C. Conductor line widths and line spacing on thick film substrates shall be a minimum of 10 mils each.

D. Conductor line widths and line spacing on thin film substrates shall be a minimum of 5 mils each except power supply lines and ground lines shall be 10 mils minimum.

E. Conductor line resistivity shall not exceed .02 ohm per square.

F. Single level construction is preferred.

G. Stacked substrate construction shall not be employed.

H. Where multilevel construction is used, the number of levels shall not exceed three.

I. The number of multilevel crossovers shall be kept to a minimum.

J. Multilevel vias shall be 15 mils x 15 mils minimum.

K. Multilevel vias shall contain metal build-up as to minimize metal steps.

L. Pad spacing under passive components must be sufficient to guarantee that short circuits will not develop when conductive attachment material is used.

3.6.3 Film Resistors.

A. Screened or deposited resistors are preferred rather than chip resistors.

B. Resistor temperature coefficient and tracking requirements must be satisfied by using appropriate materials.

C. Resistor area shall be sufficiently large to provide the required power dissipation capability after trim. Maximum resistor surface temperature shall not exceed 150 degrees C after trim.

D. Design value of thick film resistors to be trimmed shall not be less than 75 percent of nominal value.

E. Resistors shall not be trimmed down in value.

F. Resistors shall not be trimmed by use of wire bonds.

G. Resistors shall not be trimmed utilizing Blow Bar techniques employing current or voltage pulses.

3.6.4 Chip Mounting.

A. Any active chip or any passive chip with an active or metalized mounting surface shall not be mounted over conductors or resistors even though glass insulation is provided. (Single level substrate only).

B. A resistor chip or a capacitor chip with conductive end terminations may be mounted over conductors provided that the conductor run does not cross under the end terminations and that there is adequate clearance to preclude shorting.

C. Chip mounting or locating pads shall extend beyond chip outlines on all four sides a minimum of 5 mils.

D. Capacitor chips with length-to-width ratio greater than 2 to 1 shall be mounted using non-conductive epoxy under the center of the chip to increase mechanical strength.

E. Capacitor chips with areas in contact with the substrate of 500 square mils and smaller, shall be attached with conductive epoxy only.

3.6.5 Wire Bonding.

A. Wire current carrying capacity shall be adequate for the application. Maximum current in a wire shall not exceed 100,000 amperes per square centimeter.

B. The minimum wire diameter shall be 1.0 mil.

C. 10 x 10 mil minimum conductor area shall be provided for wire bonds.

D. Vias shall not be used as wire bond pads.

E. The layout design shall provide assurance that no overflow from chip mounting can impinge upon wire bonding areas.

F. Minimum spacing of 2.0 mils between wire and non-passivated areas of chip.

G. Intra-chip and inter-chip wire bonding is not permitted.

H. Interconnect wires shall not be closer than 1.0 mil to another wire, package post, die or portion of the package. Interconnect wires shall not be closer than 10 mils when measured in any direction from the bond.

I. Maximum crossover wire lengths shall be 100 mils, except wires to pinouts may be 150 mils maximum.

J. The number of crossover wires, where any single wire both originates and terminates on the substrate, shall be kept to a minimum and in no case shall exceed 10 percent of the total number of wires.

K. Strapped conductor runs shall not be used. A strapped conductor is defined as a metal run upon which a conductor has been stitch-bonded along its surface.

3.7 Workmanship. The manufacturer shall comply with the workmanship, product assurance and rework requirements of MIL-M-38510 except that delidding and opening for rework is permitted on microcircuits that have not been subjected to destructive tests.

3.7.1 Environmental Control. All fabrication, assembly and testing of hybrid microcircuits prior to precap visual inspection shall be in a Class 100,000 environment as described in Federal Standard 209.

3.7.2 Rework and Repair Provisions. All rework and repair permitted on microcircuits shall be accomplished and documented in accordance with procedures and safeguards required in MIL-STD 1772 and Appendix A of MIL-M-38510. The documents shall reflect the processes, procedures and materials to be used and shall include verification and test data. The document shall indicate that a decision to rework is made soleley by contractor personnel while a repair decision shall be made with only with the participation and concurrence of Halmatic Division. Each document shall be designated as rework or repair and shall be approved by Halmatic Division.

3.7.2.1 Delidding and Resealing. Delidding and resealing is allowed for Class B microcircuits only, and that is allowed one time only. Procedures for delidding and resealing must be qualified in accordance with the requirements of MIL-STD 1772. All rework procedures requiring delidding shall be approved by Halmatic Division prior to implementation.

3.7.2.2 Rework and Repair Operations. All rework and repair is subject to the following conditions:

A. Any temperature excursion during rework or repair shall not exceed the polymer cure temperature except in the immediate area of rework (time and temperature limits shall be specified).

B. Touch-up of the plating on the package sealing surface of delidded packages is not permitted.

C. The minimum distance between the glass to metal seals and the package sealing surface shall be at least .050 inch after final seal to prevent damage to lead seals by welding adjacent to them. (Applies to seam welding only).

D. Any device which is reworked or repaired after precap visual inspection shall be subjected to complete rescreening of Method 5008 starting with method 2017. The PIND test shall be performed only if tthis was an original requirement.

E. Replacement elements shall not be bonded onto the element they are to replace.

3.7.2.3 Rescreening. The manufacturer's rework and repair procedure shall provide for subjecting the reworked or repaired microcircuits to rescreening as well as quality conformance inspection. No PDA shall apply to rescreening such microcircuits. All successfully rescreened microcircuits shall be subjected to all Group A inspection tests on a 100 percent basis.

3.8 Manufacturing.

3.8.1 General. The manufacturer shall fabricate, screen, and test the microcircuits in accordance with requirements and processes detailed in this specification and in the referenced documents.

3.8.2 Package Preparation. The manufacturer shall use packages which meet the requirements of the detail drawing.

3.8.3 Assembly. All parts shall be attached in such manner as to preclude formation of any conductive particles which might loosen during any subsequent steps in processing and testing. Adequate clearance must be maintained for wires and for component mounting. Connections within the pakcage shall be as shown on the assembly diagram.

3.8.4 Screening. All microcircuits supplied to this specification shall be screened according to Table I in this document. Only screened microcircuits shall be used for Qualification and Quality Conformance Inspection.

3.8.5 Electrical Test. Electrical tests before screening and before burn-in are optional at the discretion of the manufacturer. If electrical tests are performed prior to screening or prior to burn-in, defective microcircuits may be excluded from the PDA. If electrical tests are omitted, then all defective microcircuits after screening shall be included in the PDA.

3.8.6 Pre-cap Visual Inspection. Prior to lidding, the assembled microcircuits shall be inspected in accordance with Method 2017 of MIL-STD- 883. Inspection shall include inspection of component attachment for particles which might loosen during processing and testing and for spacing of wires and components. After inspection by the manufacturer, the microcircuits shall be inspected by a Halmatic Division quality control representative. The manufacturer shall provide Halmatic Division five working days notification for inspection. In the event inspection by Halmatic Division is not performed within five days, the inspection may be performed by a Quality Assurance representative of the manufacturer designated by Halmatic Division.

3.8.7 Lidding and Sealing. The manufacturer shall hermetically seal the microcircuits using a lid, which when mounted, will meet the dimensional requirements specified in the detail drawing.

3.8.8 Post Sealing. Microcircuits shall be marked in accordance with 3.4 and Figure 1 or Figure 2 as applicable.

3.8.9 Burn-in. Unless otherwise specified in the detail specification, the manufacturer shall perform burn-in for 160 hours minimum at +125 degrees C, using the circuit specified in the detail drawing. In the absence of a burn-in circuit in the detail drawing, burn-in shall be performed in accordance with Method 1015 of MIL-STD 883 Test Condition A through F, as applicable. For test conditions D, E or F (where applicable), each microcircuit must be driven with an appropriate signal to simulate microcircuit applications and each microcircuit shall have maximum load applied.

3.8.9.1 Burn-in Monitoring. Microcircuits subjected to burn-in shall have their outputs monitored a minimum of two times: upon being placed into the burn-in chamber, and just prior to removal from the burn-in chamber. Monitoring shall assure that all input voltages and signals are present and that all active pins make contact. Monitoring points shall be documented in the manufacturer's burn-in procedure and schematic diagram and shall be approved by Halmatic Division.

3.8.10 Post-burn-in. The manufacturer shall perform electrical testing in accordance with the detail drawing. Results shall be recorded.

3.8.11 Test Data. Attributes summary for the electrical tests performed after burn-in test shall be retained on file by the manufacturer for 3 years.

3.8.12 PDA Lot Failure Procedure. The manufacturer shall have the option of repeating the screen once to a PDA of 5 percent or performing fault isolation on all defective microcircuits and presenting the result with rationale indicating no significant effect on lot reliability for Halmatic Division written acceptance. Halmatic Division reserves the right to make such acceptance contingent on the manufacturer's performing any designated additional testing Halmatic Division deems necessary at no additional cost.

3.8.13 Disposition of Screened Microcircuits. If the actual percent defective does not exceed the specified PDA, the lot shall be acceptable. If the actual percent defective exceeds the PDA, the lot may be resubmitted for burn-in unless the actual percent defective is greater than twice the PDA: in this event the lot is rejected outright - no resubmission allowed.

Lots may be resubmitted one time only. Resubmitted lots shall contain only microcircuits which were in the original lot. Resubmitted lots shall be kept separate from new lots and shall be inspected for all specified characteristics.

3.9 Electrical Characteristics.

3.9.1 Absolute Maximum Ratings. Absolute maximum ratings are specified in the detail drawing.

3.9.2 Electrical Requirements. Microcircuits shall meet the electrical performance characteristics specified in the detail drawing over the operating temperature range.

3.10 Environmental Conditions. Microcircuits supplied to this drawing and the detail drawing shall meet the environmental conditions indicated in MIL-STD 883, Method 5008. (Class B)

4. QUALITY ASSURANCE PROVISIONS

4.1 General. The Product Assurance Provisions of MIL-M-38510 apply. Screening, Qualification Inspection and Quality Conformance Inspection shall be in accordance with Method 5008 of MIL-STD 883, Class B, with modifications specified in this document. All circuits shall be screened in accordance with Table I.

4.1.1 Group A Inspection. Group A Inspection shall consist of the test subgroups and LTPD values shown in Method 5008 of MIL-STD 883 and as specified in the detail drawing. When the minimum required sample size exceeds the lot size, the entire lot shall be tested with accept number zero.

4.1.2 Group B Inspection. Group B Inspection shall consist of the test subgroups shown in Method 5008 of MIL-STD 883. Electrical rejects and empty packages may be used provided their construction and processing through final seal is identical to that of the circuit.

In addition, microcircuits with metallically attached substrate, when used in Subgroup 1, shall be subjected to radiographic inspection in accordance with MIL-STD 883, Method 2012 (one view in Y plane) for verification that voids in the substrate bonding do not constitute more than 50 percent of the total available attachment area.

4.1.3 Groups C and D Inspections. Groups C and D Inspections shall consist of the test subgroups shown in Method 5008 of MIL-STD 883. End point electrical parameters are specified in the detail drawing.

4.2 Failure During Qualification. If any subgroup test is failed, only one resubmission for that subgroup will be allowed with the same sample size. The only failures allowed are in tests where the sample is chosen for LTPD of 15 and the number of allowed failures depends on the sample size. If a failure occurs during the performance of the tests, Halmatic Division shall be notified immediately. Upon failure during qualification, a supplier may resubmit for qualification approval after the following conditions have been met:

A. Fault isolation is performed to establish the cause of failure for each failed circuit.

B. Corrective action, as well as supporting test data to indicate the effectiveness of the corrective action, is submitted to the satisfaction of Halmatic Division.

4.3 Failure During Quality Conformance Inspection. Upon failure during quality conformance inspection, the following procedure applies:

A. Rework: Defective microcircuits may be reworked as described in the Workmanship section of this document.

B. Rescreening: All microcircuits in the lot shall be screened to remove defective microcircuits.

C. Resubmission: The lot shall be resubmitted for all tests in quality conformance inspection. Only one resubmission is allowed. Resubmitted lots shall be kept separate from new lots and shall be clearly identified as resubmitted lots. Written concurrence from Halmatic Division shall be obtained prior to shipment.

D. Failure during resubmission: In the event of failure during resubmission, the lot shall be rejected. A summary of test results shall be forwarded to Halmatic Division.

4.4 Data Retention.

4.4.1 Group A. Attributes summary for Group A electrical tests shall be retained on file by the manufacturer for 3 years.

4.4.2 Groups B, C and D. The manufacturer is required to retain test data for a period of not less than 3 years from the date of shipment.

4.4.3 Screening Test Data. Attributes summary for the electrical tests performed after burn-in test shall be retained on file by the manufacturer for 3 years.

4.4.4 Documentation. Upon completion of qualification tests, the manufacturer shall generate a test report including data sheets and documentation for the actual construction of the microcircuits used in Qualification Inspection. The sample microcircuits used in the testing shall be delivered with the test report.

4.5 Fault Isolation on Returned Microcircuits. The manufacturer shall be responsible for performing fault isolation upon request by Halmatic Division at no additional cost for any circuit returned within 12 months of date of delivery and determined to be the manufacturer's responsibility.

4.6 Method of Examination and Test.

4.6.1 Voltage and Current. Unless otherwise specified, all voltages given are referenced to the circuit ground terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

4.6.2 Cooldown Procedure. When microcircuits are tested at 25 degrees C after operating life or burn-in, they shall be cooled until the case is at room temperature prior to removal of the bias. Alternately, the bias may be removed during cooling if the case temperature is reduced to room temperature within 30 minutes.

4.6.3 Test Tolerances. The tabulated tolerances apply unless otherwise stated in the detail drawing.

IMPOSED CONDITION	TOLERANCE
Temperature	+,- 5 degrees C
Power supply voltage	+,- 1 percent
Bias voltage	+,- 1 percent
Breakdown voltage	+,- 1 percent
Input signals:	
Voltage	+,- 1 percent
Current	+,- 1 percent
Pulse width	+,- 5 percent or 1 nanosecond, whichever is greater
Repetition rate	+,- 10 percent
Frequency	+,- 10 percent

OUTPUT LOAD	TOLERANCE
Current: maximum, worst case	-
Resistors (non-inductive)	+,- 1 percent
Capacitors	+,- 5 percent or +,- 1 picofarad, whichever is greater
Inductors	+,- 5 percent or +,- 5 microhenry, whichever is greater

MEASUREMENTS	TOLERANCE
DC parameters	+,- 1 percent
Pulses	+,- 5 percent or 1 nanosecond, whichever is greater

5. PREPARATION FOR DELIVERY

5.1 Preservation - Packaging and Packing. Microcircuits shall be prepared for delivery in accordance with DOD-STD-1686 and MIL-M-38510 Level C.

5.2 Packaging. Microcircuits shall be individually packaged in cardboard, anti-static type carrier, in an appropriate size for the individual hybrid microcircuit.

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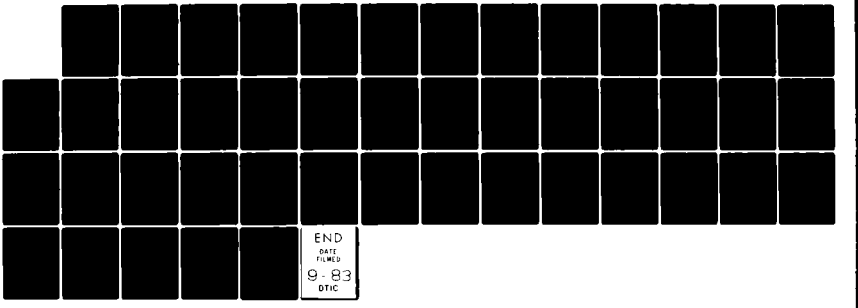

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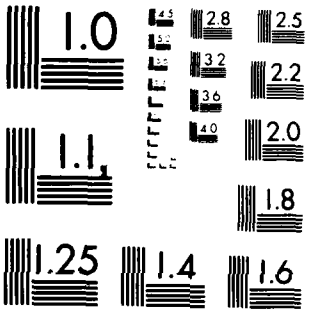


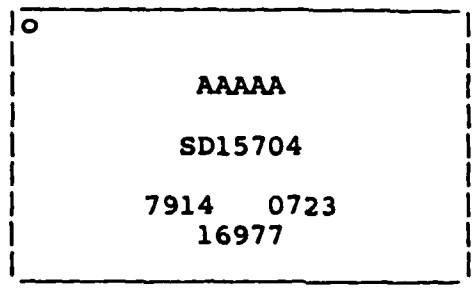
TABLE I - SCREENING PROCEDURE

STEP	TEST (Note 1)	MIL-STD 883 METHOD	CONDITION	COMMENTS
I	Pre-seal burn-in	1030		Optional
II	Internal Visual (Precap)	2017	B	
III	High Temperature Storage	1008	C	24 hours minimum
IV	Temperature Cycling	1010	C	
V	Constant Acceleration or Mechanical Shock	2001 2002	(Note 2) B	Y1 plane only
VI	Pre burn-in electrical			Optional
VII	Burn-in (Note 3)	1015	C	160 hours minimum
VIII	Electrical Parameters (Note 3)			
IX	Seal (Note 4) a. Fine b. Gross	1014	 A or B C or D	
X	External Visual	2009		Figure 1 in detail drawing

NOTES:

1. Notes of MIL-STD 883, Method 5008 are applicable.
2. Packages with inner seal perimeter of less than 2.0 inches: Condition E. Packages with inner seal perimeter of 2.0 inches or greater: Condition A.
3. Refer to the detail specification for additional conditions and requirements for the test.
4. Seal test may be performed in any sequence after Step IV. The order of performing the fine and gross seal test may be exchanged when fluorocarbon gross method, test condition C, is used.

PIN 1
Index Point



NOTES: Values shown are examples only

Line 1: Manufacturer's name or symbol

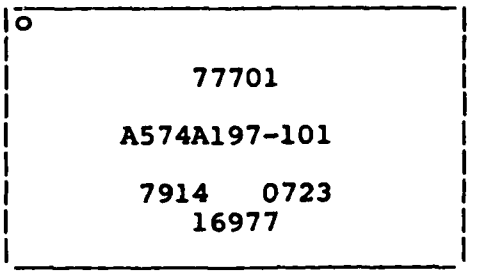
Line 2: Manufacturer's unique part number

Line 3: Date code and lot number

Line 4: Serial number

FIGURE 1 MARKING PLACEMENT - Group I Microcircuits

PIN 1
Index Point



NOTES: Values shown are examples only (except line 1)

Line 1: Bendel Halmatic FSCM number

Line 2: Halmatic part number = drawing number + dash number

Line 3: Date code and lot number

Line 4: Serial number

FIGURE 2 MARKING PLACEMENT - Group II Microcircuits

Appendix B

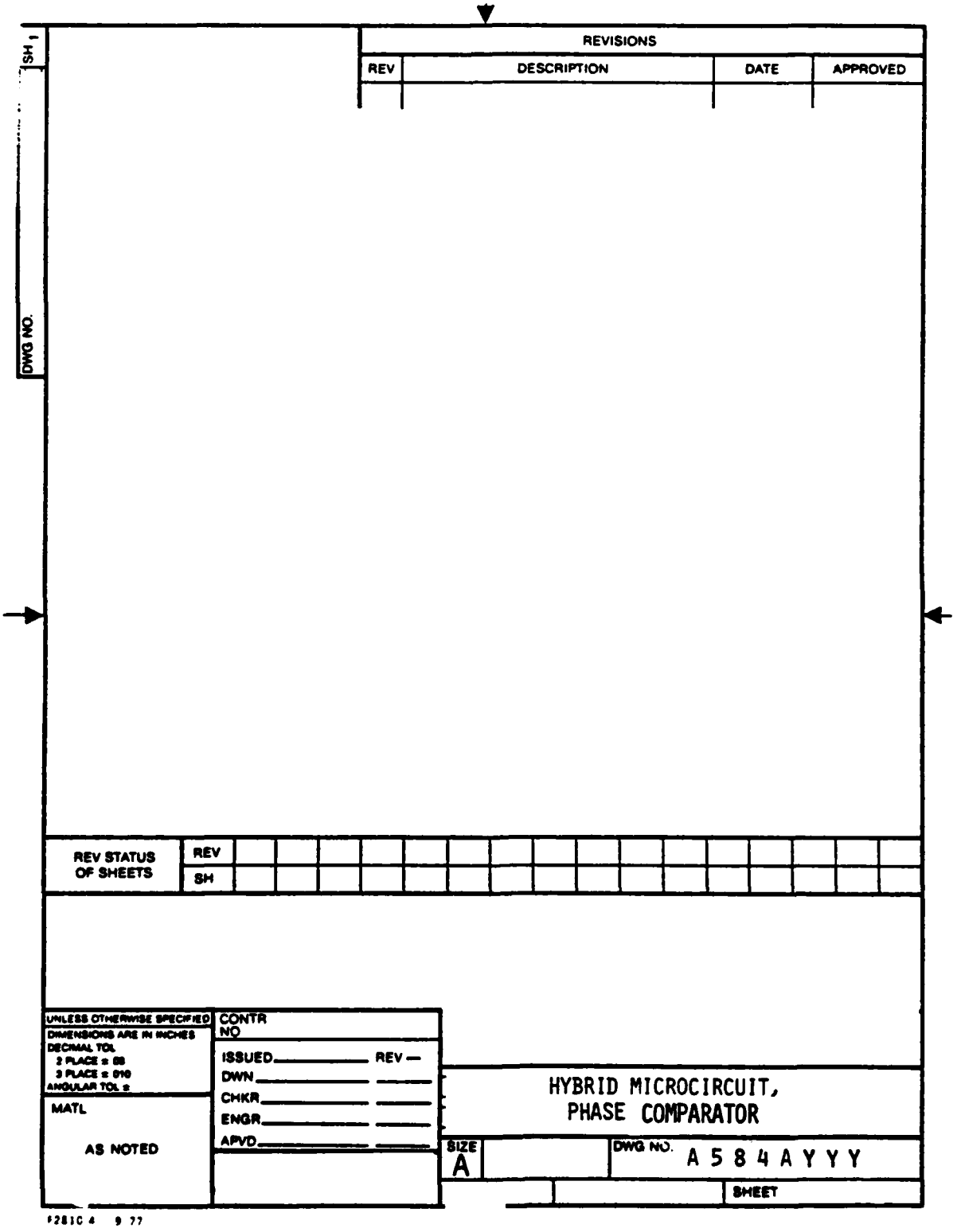
Sample

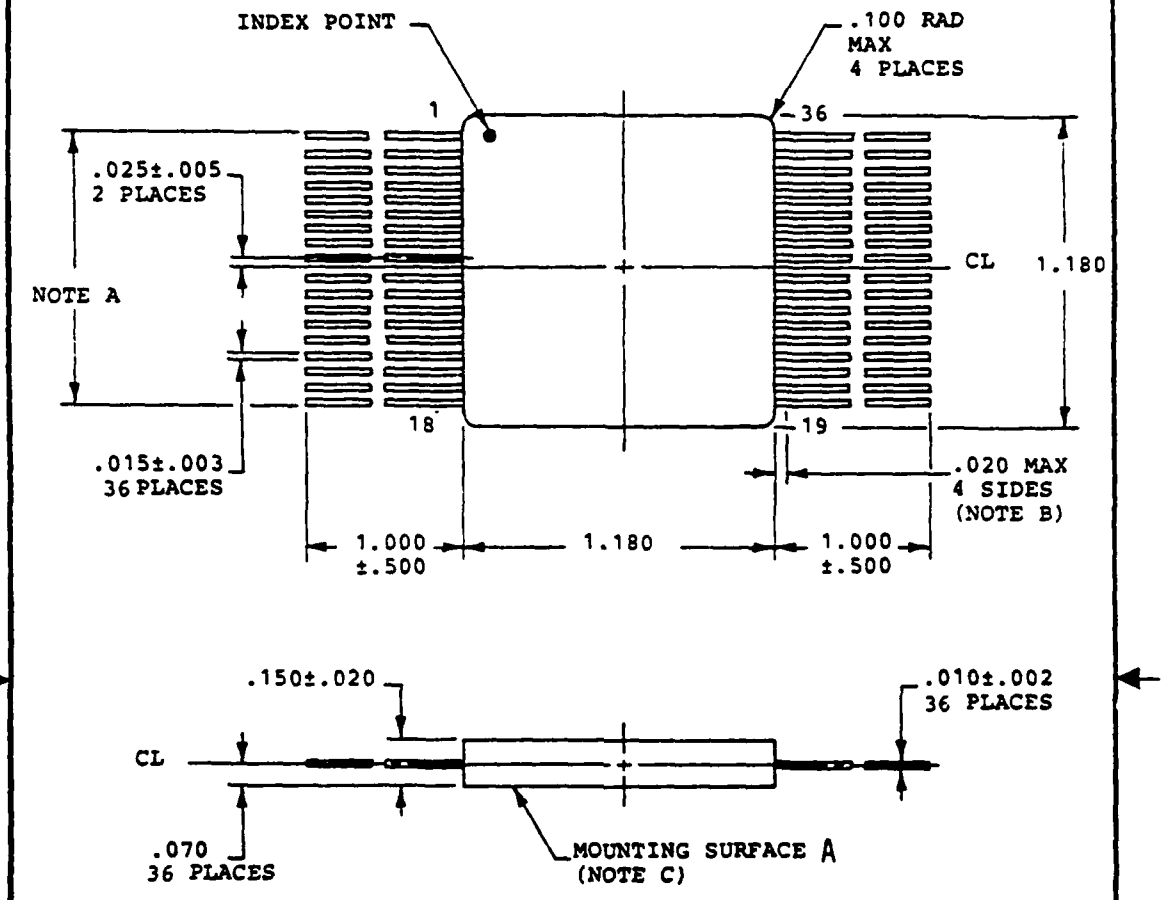
DETAIL SPECIFICATION

FOR A

HYBRID MICROCIRCUIT

A584AYYY


SH 1
DWG NO.
REVISIONS
REV
DESCRIPTION
DATE
APPROVED
REV STATUS OF SHEETS
REV
SH
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
DECIMAL TOL
2 PLACE ± 08
3 PLACE ± 010
ANGULAR TOL ±
MATL
AS NOTED
CONTR NO
ISSUED
REV —
DWN
CHKR
ENGR
APVD
HYBRID MICROCIRCUIT,
PHASE COMPARATOR
SIZE
A
DWG NO.
A 5 8 4 A Y Y Y
SHEET
F281C 4 9 77



NOTES:

A. 18 LEADS EQUALLY SPACED AT 0.050 ±0.005 TOLERANCES NONCUMULATIVE, LOCATE SYMMETRICALLY FROM CL INDICATED (BOTH SIDES).

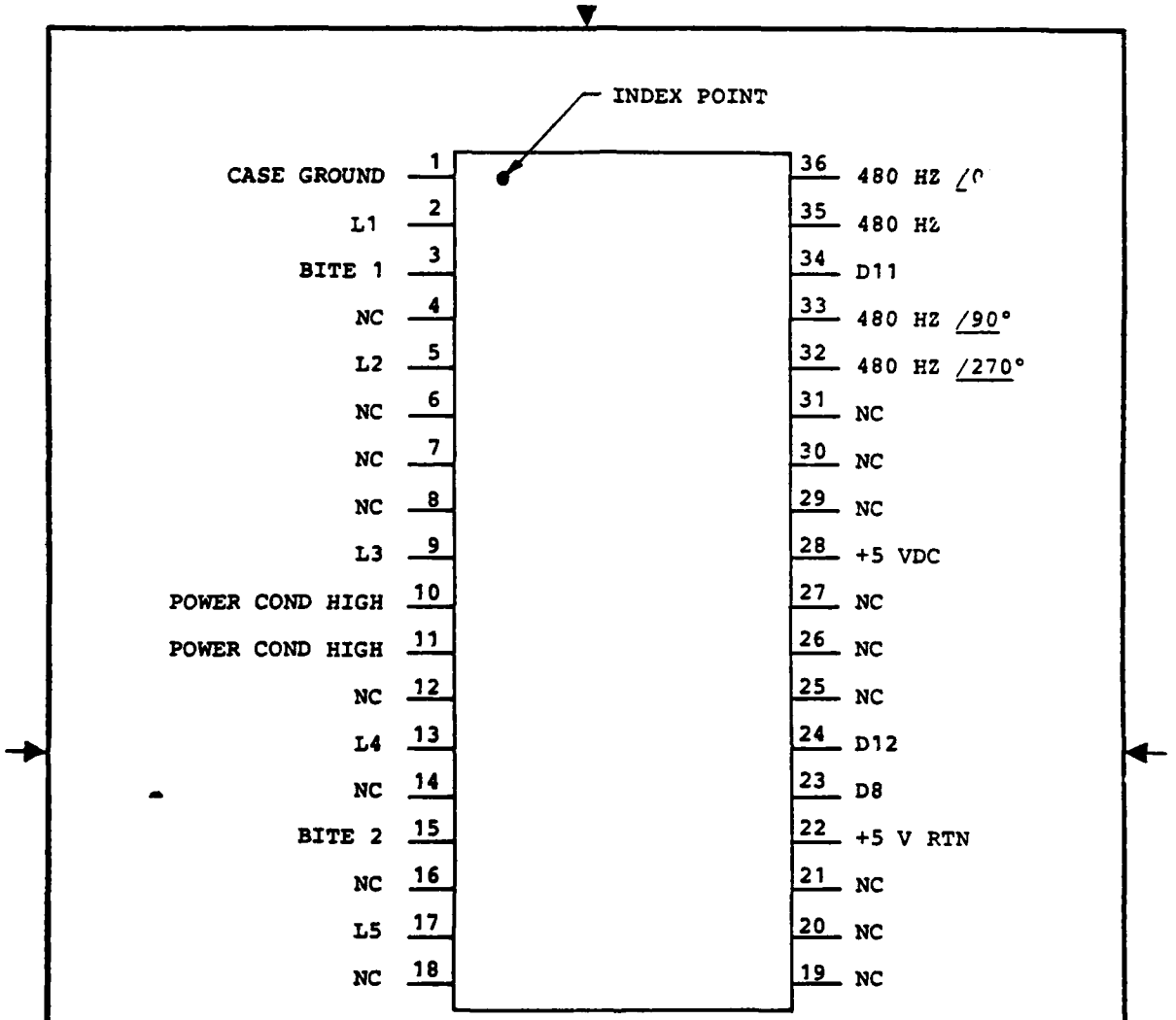
B. SPECIFIED DIMENSION APPLIES TO TOP COVER ONLY, INCLUDING EXTRUDED PREFORM MATERIAL AND/OR COVER OVERLAP.

C. SURFACES MARKED A TO BE FLAT WITHIN 0.005 TOTAL INDICATOR READING.

FIGURE 1

DWN	SEE SH 1	SIZE A	DWG NO A584AYYY	REV
ISSUED	SEE SH 1			SHEET

F2811D 9.77

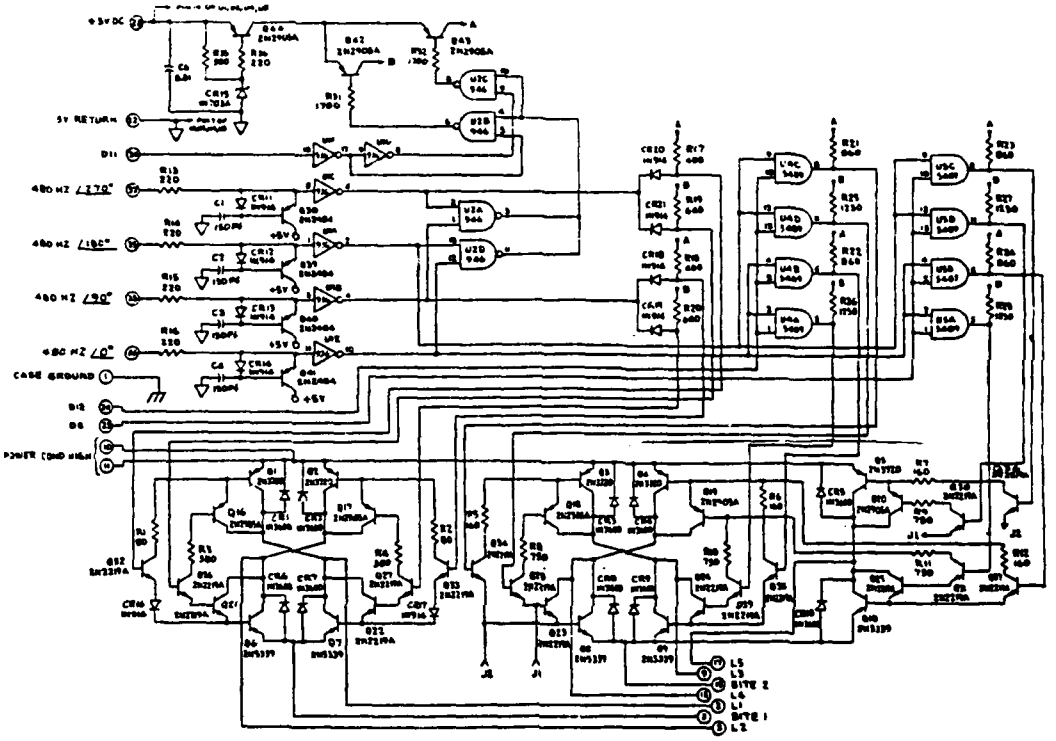


NC = NO CONNECTION, NOT TO BE USED INTERNALLY

CONNECTION DIAGRAM - TOP VIEW
FIGURE 2

DWN	SEE SH 1	SIZE A		DWG NO A584AYYY	REV
ISSUED	SEE SH 1			SHEET	

F2811D 9.77



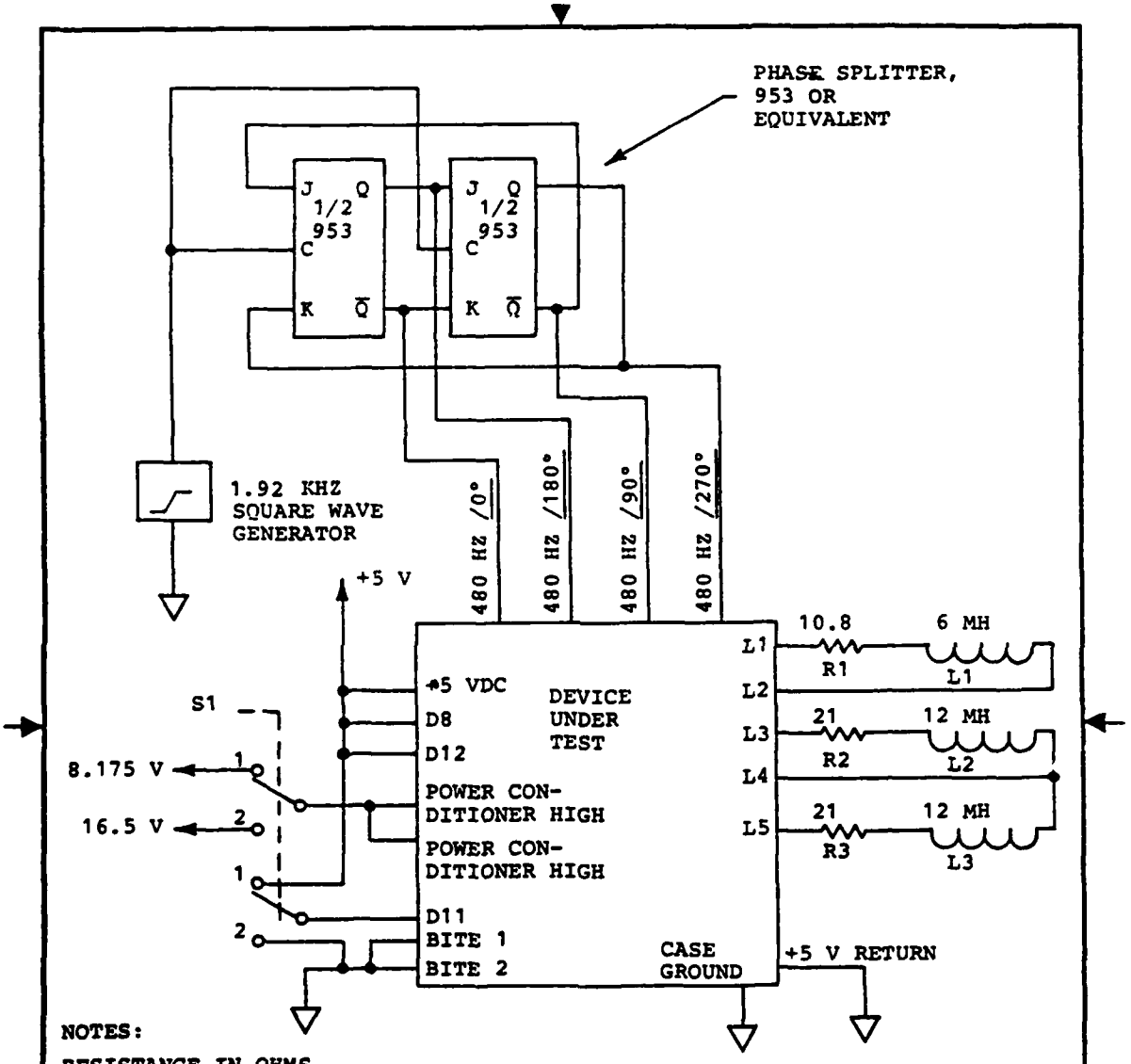
COMPONENTS ARE DETAILED IN TABLES II, III AND IV.

SCHEMATIC DIAGRAM

FIGURE 3

DWN	SEE SH 1	SIZE A		DWG NO A 5 8 4 A Y Y Y	REV
ISSUED	SEE SH 1			SHEET	

F2811D 9 77



NOTES:

RESISTANCE IN OHMS.

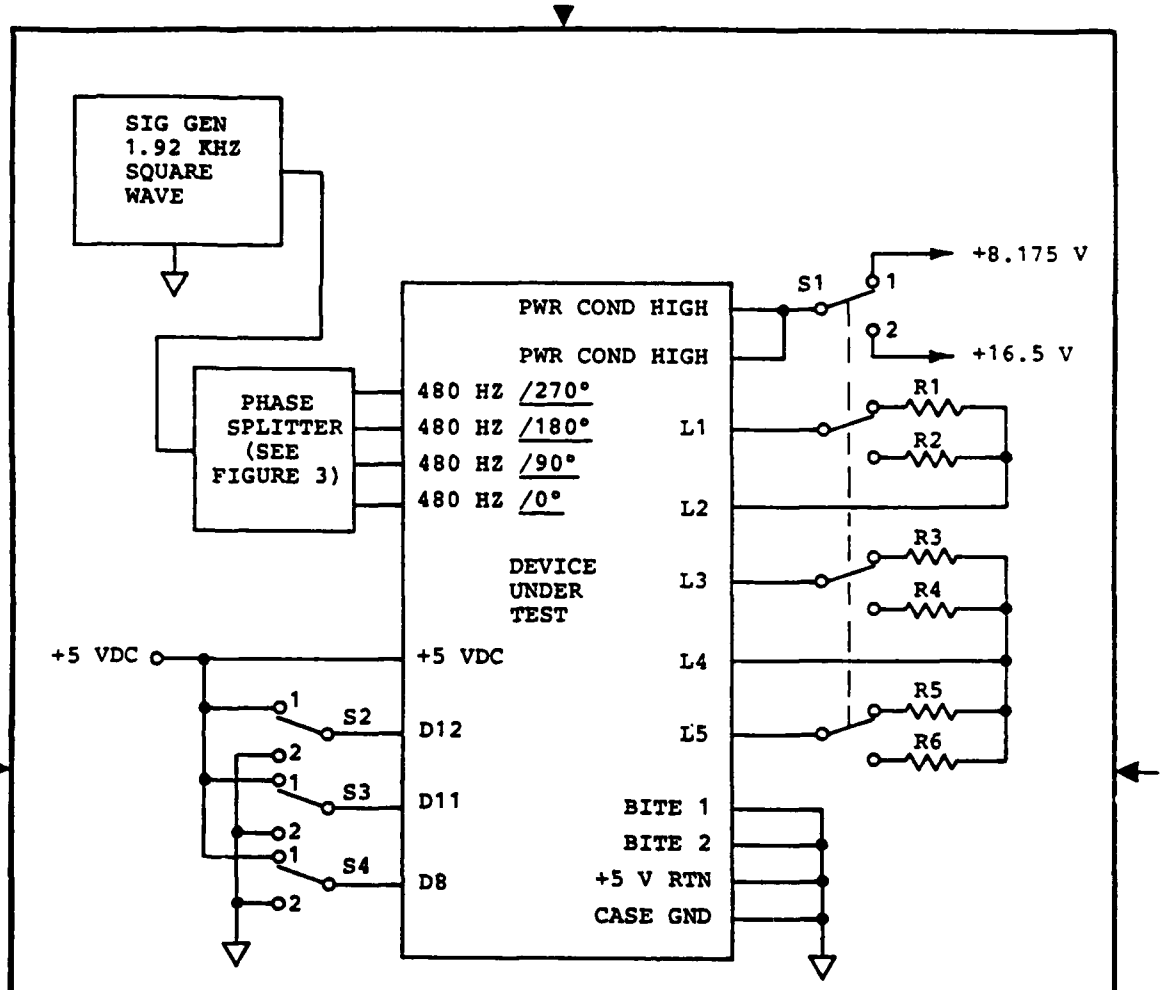
R1 = 10.8 OHMS ±2 PERCENT, 25 WATTS
R2 = R3 = 21 OHMS ±2 PERCENT, 12.5 WATTS
L1 = 6 MILLIHENRIES ±10 PERCENT AT 1.6 AMPERES RMS
L2 = L3 = 12 MILLIHENRIES ±10 PERCENT AT 0.8 AMPERE RMS
SWITCH S1: POSITION 1 FOR 164 HOURS, POSITION 2 FOR 4 HOURS.

BURN-IN AND OPERATING LIFE CIRCUIT

FIGURE 4

DWN	SEE SH 1	SIZE A	DWG NO A584AYYY	REV
ISSUED	SEE SH 1		SHEET	

F2811D 9.77



NOTES:

R1 = 47 OHMS ±5 PERCENT , 10 WATTS MINIMUM.
R2 = 12 OHMS ±5 PERCENT , 25 WATTS MINIMUM.
R3, R5 = 95 OHMS ±5 PERCENT , 5 WATTS MINIMUM.
R4, R6 = 24 OHMS ±5 PERCENT , 15 WATTS MINIMUM.

TEST CIRCUIT

FIGURE 5A

DWN	SEE SH 1	SIZE A		DWG NO A584AYYY	REV
ISSUED	SEE SH 1			SHEET	

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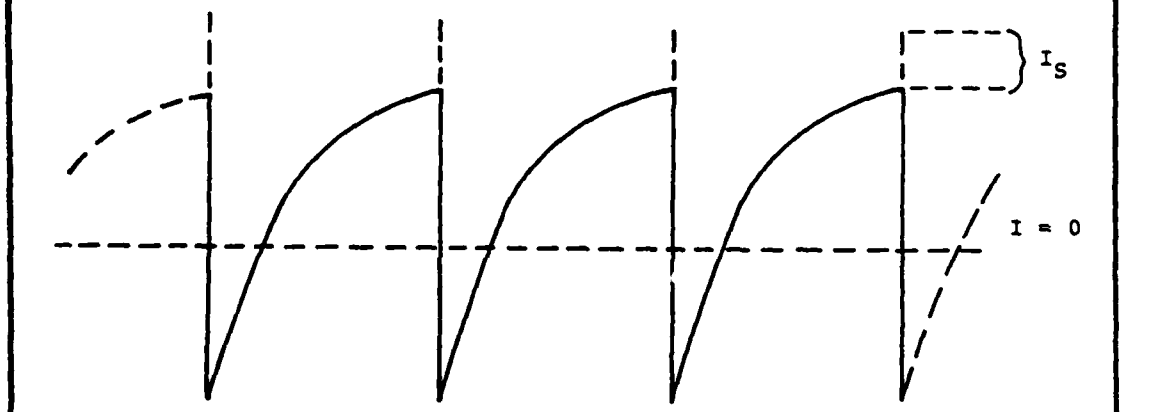

TYPICAL CURRENT IN
POWER CONDITIONER HIGH LINE

FIGURE 5B

DWN	SEE SH 1	SIZE A		DWG NO A 5 8 4 A Y Y Y	REV
ISSUED	SEE SH 1			SHEET	

F2811D 9.77

TABLE I

PART NUMBER	MANUFACTURED ONLY FOR HALMATIC DIVISION BY THE FOLLOWING:
A584AYYY-101	ACCORD AIRCRAFT COMPANY MICROELECTRONICS PRODUCT DIVISION HICKSVILLE, CALIFORNIA (CODE IDENTIFICATION NUMBER 10150)
	GENERAL CIRCUITS COMPANY AEROSPACE ELECTRONICS PRODUCTS DEPARTMENT QUINCY, NEW YORK (CODE IDENTIFICATION NUMBER 10057)
	TELECONS MICROELECTRONICS MEADOWBANK, CALIFORNIA (CODE IDENTIFICATION NUMBER 02029)

DWN SEE SH 1	SIZE A		DWG NO A 5 8 4 A Y Y Y	REV
ISSUED SEE SH 1				SHEET

F2811D 9.77

TABLE II

COMPONENTS LIST: RESISTORS

REFERENCE DESIGNATION (FIGURE 3)	RESISTANCE (OHMS)	TOLERANCE 1/ (± PERCENT)	POWER 2/ DISSIPATION (MILLIWATTS)	MAXIMUM TEMPERATURE COEFFICIENT 3/ (± PPM/DEGREE C)
R1	80	10	0	200
R2	80	10	0	200
R3	380	10	340	200
R4	380	10	340	200
R5	160	10	0	200
R6	160	10	0	200
R7	160	10	0	200
R8	750	10	170	200
R9	750	10	170	200
R10	750	10	170	200
R11	750	10	170	200
R12	160	10	0	200
R13	220	10	14	200
R14	220	10	14	200
R15	220	10	14	200
R16	220	10	14	200
R17	400	20	62.5	200
R18	400	20	62.5	200
R19	640	10	20	200
R20	640	10	20	200
R21	860	20	29	200
R22	860	20	29	200
R23	860	20	29	200
R24	860	20	29	200
R25	1250	20	11.5	200
R26	1250	20	11.5	200
R27	1250	20	11.5	200

DWN SEE SH 1	SIZE A		DWG NO A 5 8 4 A Y Y Y	REV
ISSUED SEE SH 1				SHEET

F28110 9.77

TABLE II(CONTINUED)

COMPONENTS LIST: RESISTORS

REFERENCE DESIGNATION (FIGURE 3)	RESISTANCE (OHMS)	TOLERANCE 1/ (± PERCENT)	POWER 2/ DISSIPATION (MILLIWATTS)	MAXIMUM TEMPERATURE COEFFICIENT 3/ (± PPM/DEGREE C)
R28	1250	20	11.5	200
R29	NOT USED			
R30	NOT USED			
R31	1700	10	6.8	200
R32	1700	10	6.8	200
R33	NOT USED			
R34	NOT USED			
R35	300	10	17	200
R36	220	10	14	200

NOTES:

1/ TOLERANCES INCLUDE THE EFFECTS OF INITIAL SET AND ANY COMBINATION OF OPERATION AND LOADING. TOLERANCES APPLY OVER THE FULL LIFE EXPECTANCY OF THE HYBRID CIRCUIT.

2/ RESISTOR DISSIPATIONS INDICATED ARE BASED ON CIRCUIT APPLICATION. A SAFETY FACTOR OF AT LEAST 2 TO 1 IS REQUIRED ON POWER RATING.

3/ AVERAGED OVER THE TEMPERATURE RANGE OF T_C = -55 TO +25 DEGREES C AND T_C = +25 TO +125 DEGREES C.

DWN SEE SH 1	SIZE A		DWG NO A 5 8 4 A Y Y Y	REV
ISSUED SEE SH 1	SCALE NONE			SHEET 10

TABLE III

COMPONENTS LIST: CAPACITORS

REFERENCE DESIGNATION (FIGURE 3)	CAPACITANCE (MICROFARADS)	TOLERANCE 1/ (± PERCENT)	APPLIED 2/ VOLTAGE (VOLTS)	MAXIMUM TEMPERATURE COEFFICIENT 3/ (± PPM/DEGREE C)
C1	150 PF	10	5.5	1500
C2	150 PF	10	5.5	1500
C3	150 PF	10	5.5	1500
C4	150 PF	10	5.5	1500
C5	NOT USED			
C6	0.01	10	5.5	1500

NOTES:

1/ TOLERANCES INCLUDE THE EFFECTS OF INITIAL SET AND ANY COMBINATION OF OPERATION AND LOADING. TOLERANCES APPLY OVER THE FULL LIFE EXPECTANCY OF THE HYBRID CIRCUIT.

2/ CAPACITOR VOLTAGES INDICATED ARE BASED ON CIRCUIT APPLICATION. A SAFETY FACTOR OF AT LEAST 2 TO 1 IS REQUIRED ON VOLTAGE.

3/ AVERAGED OVER THE TEMPERATURE RANGE OF T_C = -55 TO +25 DEGREES C AND T_C = +25 TO +125 DEGREES C.

DWN SEE SH 1	SIZE A		DWG NO A584AYYY	REV
ISSUED SEE SH 1	SCALE NONE		SHEET 11	

TABLE IV

COMPONENTS LIST: SEMICONDUCTOR DEVICES

DIODES

REFERENCE DESIGNATION (FIGURE 3)	GENERIC 1/ EQUIVALENT	
CR1 2/	1N3600	P ≤ 10
CR2 2/	1N3600	
CR3 2/	1N3600	
CR4 2/	1N3600	
CR5 2/	1N3600	
CR6 2/	1N3600	
CR7 2/	1N3600	
CR8 2/	1N3600	
CR9 2/	1N3600	
CR10 2/	1N3600	
CR11	1N3600	
CR12	1N3600	
CR13	1N3600	
CR14	1N3600	
CR15	1N703A	V_Z=3.0 V ±5 PERCENT, AT I_Z=2 MA TC=-.15 PERCENT/DEGREE C MAX, P_D= 52 MW
CR16	1N3600	P ≤ 10
CR17	1N3600	
CR18	1N3600	
CR19	1N3600	
CR20	1N3600	
CR21	1N3600	

TABLE III

COMPONENTS LIST: CAPACITORS

REFERENCE DESIGNATION (FIGURE 3)	CAPACITANCE (MICROFARADS)	TOLERANCE 1/ (± PERCENT)	APPLIED 2/ VOLTAGE (VOLTS)	MAXIMUM TEMPERATURE COEFFICIENT 3/ (± PPM/DEGREE C)
C1	150 PF	10	5.5	1500
C2	150 PF	10	5.5	1500
C3	150 PF	10	5.5	1500
C4	150 PF	10	5.5	1500
C5	NOT USED			
C6	0.01	10	5.5	1500

NOTES:

1/ TOLERANCES INCLUDE THE EFFECTS OF INITIAL SET AND ANY COMBINATION OF OPERATION AND LOADING. TOLERANCES APPLY OVER THE FULL LIFE EXPECTANCY OF THE HYBRID CIRCUIT.

2/ CAPACITOR VOLTAGES INDICATED ARE BASED ON CIRCUIT APPLICATION. A SAFETY FACTOR OF AT LEAST 2 TO 1 IS REQUIRED ON VOLTAGE.

3/ AVERAGED OVER THE TEMPERATURE RANGE OF T_C = -55 TO +25 DEGREES C AND T_C = +25 TO +125 DEGREES C.

DWN SEE SH 1	SIZE A		DWG NO A 5 8 4 A Y Y Y	REV
ISSUED SEE SH 1	SCALE NONE			SHEET 11

TABLE IV

COMPONENTS LIST: SEMICONDUCTOR DEVICES

DIODES

REFERENCE DESIGNATION (FIGURE 3)	GENERIC 1/ EQUIVALENT	
CR1 2/	1N3600	P ≤ 10
CR2 2/	1N3600	
CR3 2/	1N3600	
CR4 2/	1N3600	
CR5 2/	1N3600	
CR6 2/	1N3600	
CR7 2/	1N3600	
CR8 2/	1N3600	
CR9 2/	1N3600	
CR10 2/	1N3600	
CR11	1N3600	
CR12	1N3600	
CR13	1N3600	
CR14	1N3600	
CR15	1N703A	V_Z=3.0 V ±5 PERCENT, AT I_Z=2 MA TC=-.15 PERCENT/DEGREE C MAX, P_D= 52 MW
CR16	1N3600	P ≤ 10
CR17	1N3600	
CR18	1N3600	
CR19	1N3600	
CR20	1N3600	
CR21	1N3600	

DWN SEE SH 1	SIZE A	DWG NO A584AYYY	REV	
ISSUED SEE SH 1			SHEET	

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TABLE IV (CONTINUED)

COMPONENTS LIST: SEMICONDUCTOR DEVICES

TRANSISTORS

REFERENCE DESIGNATION (FIGURE 3)	GENERIC 1/ EQUIVALENT	
Q1 2/	2N3720	V_{CE}(SAT) = 0.150 V MAX AT I_C = 500 MA, I_B = 60 MA, T_A = 25 DEGREES C; V_{BE}(SAT) = 1.0 V MAX AT I_C/I_B = 10, I_B = 86 MA, T_A = 25 DEGREES C, P_W MAX = 650 MW
Q2 2/	2N3720	
Q3 2/	2N3720.	
Q4 2/	2N3720	
Q5 2/	2N3720	
Q6 2/	2N5339	V_{CE}(SAT) = 0.075 V MAX AT I_C = 500 MA, I_B = 60 MA, T_A = 25 DEGREES C; V_{BE}(SAT) = 0.9 V MAX AT I_C/I_B = 10, I_B = 86 MA, T_A = 25 DEGREES C, P_W MAX = 650 MW
Q7 2/	2N5339	
Q8 2/	2N5339	
Q9 2/	2N5339	
Q10 2/	2N5339	
Q11	NOT USED	
Q12	NOT USED	
Q13	NOT USED	
Q14	NOT USED	
Q15	NOT USED	
Q16	2N2905A	P_W MAX = 30 MW
Q17	2N2905A	
Q18	2N2905A	
Q19	2N2905A	
Q20	2N2905A	

TABLE IV (CONTINUED)

COMPONENTS LIST: SEMICONDUCTOR DEVICES

TRANSISTORS (CONTINUED)

REFERENCE DESIGNATION (FIGURE 3)	GENERIC 1/ EQUIVALENT	
Q21	2N2219A	P_W MAX = 30 MW
Q22	2N2219A	
Q23	2N2219A	
Q24	2N2219A	
Q25	2N2219A	
Q26	2N2219A	
Q27	2N2219A	
Q28	2N2219A	
Q29	2N2219A	P_W MAX = 30 MW
Q30	2N2219A	
Q31	2N2219A	
Q32	2N2219A	
Q33	2N2219A	
Q34	2N2219A	
Q35	2N2219A	
Q36	2N2219A	
Q37	2N2219A	
Q38	2N2484	P_W < 10 MW
Q39	2N2484	
Q40	2N2484	
Q41	2N2484	
Q42	2N2905A	V_{CE}(SAT) = 0.15 V MAX AT I_C/I_B = 10, I_C = 50 MA, P_W MAX = 40 MW
Q43	2N2905A	
Q44	2N2905A	

DWN	SEE SH 1	SIZE A		DWG NO A584AYYY	REV
ISSUED	SEE SH 1			SHEET	

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TABLE IV (CONTINUED)

COMPONENTS LIST: SEMICONDUCTOR DEVICES

INTEGRATED CIRCUITS

REFERENCE DESIGNATION (FIGURE 3)	GENERIC 1/ EQUIVALENT
U1	936
U2	946
U3	NOT USED
U4	5409
U5	5409

NOTES:

1/ UNLESS OTHERWISE INDICATED, NORMAL DEVICE CHARACTERISTICS (AS INDICATED ON REGISTERED EIA, JAN DATA SHEETS, ETC) APPLY.

FOR MICROCIRCUITS, THE PIN DESIGNATIONS SHOWN ON THE SCHEMATIC DIAGRAM (FIGURE 3) REFLECT THE USE OF TO-99 PACKAGES. WHEN CONVERTING TO THE HYBRID CIRCUIT, THE INTERCONNECTIONS SHALL BE COMPATIBLE WITH THE SCHEMATIC DIAGRAM.

2/ BONDING WIRE FOR Q1 THROUGH Q10 AND CR1 THROUGH CR10 SHOULD BE CAPABLE OF 5.0 AMPERES PEAK. TRANSISTORS Q1 THROUGH Q10 SHALL BE CAPABLE OF CONDUCTING 5 AMPERES. THE POWER CONDITION HIGH SHOULD BE CAPABLE OF 3.9 AMPERES PEAK. BITE 1 AND BITE 2 SHOULD BE CAPABLE OF 2.7 AMPERES PEAK.

TABLE V

ELECTRICAL PERFORMANCE CHARACTERISTICS

CHARACTERISTIC	SYMBOL 1/	LIMITS MIN	LIMITS MAX	UNITS
OUTPUT VOLTAGE, RUN MODE	V_{O1}	15.875	16.325	V_{PP}
OUTPUT VOLTAGE, START MODE	V_{O2}	28.3	30.5	V_{PP}
OUTPUT OFFSET (RUN MODE)	V_{OS}		±50	MVDC
TRANSITION TIME	T_{rf}	0	35	uSEC
†OUTPUT VOLTAGE DRIFT -20 TO +100 DEGREES C	ΔV_{01}	--	±0.153	V_{P-P}
†OUTPUT VOLTAGE DRIFT -55 TO -20 DEGREES C	ΔV_{01}	--	±0.165	V_{P-P}
MODULE POWER DISSIPATION				
START MODE (t <90 SEC.)	$P_{DISS(S)}$	--	7.3	W
RUN MODE (t >90 SEC.)	$P_{DISS(R)}$	--	2.2	W
POWER SUPPLY CURRENT DRAIN	$I_{P.S.}$			
+5VDC		--	160	MA
+16.5VDC (START) PEAK		--	4.0	A
+16.5VDC (START) (DC)		--	1.8	A
+8.175VDC (RUN) PEAK		--	1.8	A
+8.175VDC (RUN) (DC)		--	0.7	A

† DRIFT LIMITS WITH CONSTANT POWER SUPPLY VOLTAGE

1/ SEE 3.3 FOR DEFINITIONS

TABLE VI

GROUP A INSPECTION

SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
SUBGROUP 1	T_C = +25 DEGREES C			
I_{IL}	V_{IN} = GND			
	480 HZ /0°		-1.8	MA
	480 HZ /90°		-1.8	MA
	480 HZ /180°		-1.8	MA
	480 HZ /270°		-1.8	MA
I_{IH}	V_{IN} = +2.4 VOLTS DC			
	480 HZ /0°		40	µA
	480 HZ /90°		40	µA
	480 HZ /180°		40	µA
	480 HZ /270°		40	µA
V_{OL}	I_{OL} = -1.8 MA			
	L1		+0.4	VOLT
	L2		+0.4	VOLT
	L3		+0.4	VOLT
	L4		+0.4	VOLT
	L5		+0.4	VOLT
V_{OH}	I_{OH} = 40 µA			
	L1	+2.4		VOLTS
	L2	+2.4		VOLTS
	L3	+2.4		VOLTS
	L4	+2.4		VOLTS
	L5	+2.4		VOLTS
SUBGROUP 2	T_C = +125 DEGREES C			
TESTS, TEST CONDITIONS, AND LIMITS: SAME AS SUBGROUP 1.				
SUBGROUP 3	T_C = -55 DEGREES C			
TESTS, TEST CONDITIONS, AND LIMITS: SAME AS SUBGROUP 1.				

DWN SEE SH 1	SIZE A		DWG NO A 5 8 4 A Y Y Y	REV
ISSUED SEE SH 1	SCALE NONE		SHEET 17	

TABLE VI (CONTINUED)
GROUP A INSPECTION

SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
SUBGROUP 4 (CONTINUED)				
f_1	SWITCH: S1 S2 S3 S4 POSITION: 1 1 1 1 DECREASE THE FREQUENCY OF THE SIGNAL GENERATOR UNTIL DISTORTION IS NOTED IN THE WAVEFORM ACROSS R1. RECORD FREQUENCY.	--	860	HERTZ
TEST 1	SWITCH: S1 S2 S3 S4 POSITION: 2 1 2 1 SIGNAL GENERATOR OFF. MEASURE BETWEEN L1, L2, L3, L4 AND L5 TO GROUND.	--	0	Vpp
TEST 2	SWITCH: S1 S2 S3 S4 POSITION: 1 1 1 1 DECREASE ±5 VOLTS DC SUPPLY UNTIL THERE IS NOT OUTPUT ACROSS R1. MEASURE SUPPLY VOLTAGE.	3.122	4.5	VDC
SUBGROUP 5	T_C = +125 DEGREES C			
ΔV_{O1}	MEASURE V_{O1} IN ACCORDANCE WITH SUBGROUP 4. DIFFERENCE IN V_{O1} READINGS.	--	±0.1526	Vpp
V_{OS}	SAME AS SUBGROUP 4		±50	MVLC
V_{O2}	SAME AS SUBGROUP 4	28.3	30.5	Vpp
f1	SAME AS SUBGROUP 4		950	
TEST 1	SAME AS SUBGROUP 4	SAME AS SUBGROUP 4		
TEST 2	SAME AS SUBGROUP 4	SAME AS SUBGROUP 4		

DWN SEE SH 1	SIZE A		DWG NO A584AYYY	REV
ISSUED SEE SH 1	SCALE NONE		SHEET 19	

TABLE VI (CONTINUED)

GROUP A INSPECTION

SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
SUBGROUP 6	T_C = -55 DEGREES C			
ΔV_{O1}	SAME AS SUBGROUP 5		±0.165	Vpp
V_{OS}	SAME AS SUBGROUP 4		±50	MVDC
V_{O2}	SAME AS SUBGROUP 4	28.3	30.5	Vpp
f1	SAME AS SUBGROUP 4		950	
TEST 1	SAME AS SUBGROUP 4	SAME AS SUBGROUP 4		
TEST 2	SAME AS SUBGROUP 4	SAME AS SUBGROUP 4		
SUBGROUP 7	T_C = +25 DEGREES C VERIFY CIRCUIT FUNTION REQUIREMENTS OF TABLE V			
SUBGROUP 8A	T_C = +125 DEGREES C TESTS, TEST CONDITIONS, AND LIMITS: SAME AS SUBGROUP 7.			
SUBGROUP 8B	T_C = -55 DEGREES C TESTS, TEST CONDITIONS, AND LIMITS: SAME AS SUBGROUP 7.			
SUBGROUP 9	T_C = +25 DEGREES C			
T_{rf}	SAME AS V_{O1}, SUBGROUP 4	0	35	USEC
I_S	FIGURE 4, TEST WITH S1 IN BOTH POSITIONS	0	1000	MA
SUBGROUP 10	T_C = +125 DEGREES C TESTS, TEST CONDITIONS, AND LIMITS: SAME AS SUBGROUP 9.			
SUBGROUP 11	T_C = -55 DEGREES C TESTS, TEST CONDITIONS, AND LIMITS: SAME AS SUBGROUP 9.			

Page 110 deleted.

NOTES.

HYBRID MICROCIRCUIT, PHASE COMPARATOR;

1. GENERAL.
THIS DRAWING COVERS THE REQUIREMENTS FOR A MICRCIRCUIT. IN ADDITION TO THE DETAIL REQUIREMENTS OF THIS DRAWING. THE MICROCIRCUIT SHALL MEET THE REQUIREMENTS OF Y125A18.0 (GENERAL SPECIFICATION FOR HYBRID MICROCIRCUITS), EXCEPT AS NOTED HERE.

1.1 THE MICROCIRCUIT SHALL BE DESIGNED AND MANUFACTURED FOR A MINIMUM LIFE EXPECTANCE OF 10 YEARS UNDER ANY COMBINATION OF STORAGE OR OPERATIONAL USAGE.

1.2 MANUFACTURING FACILITIES APPEARING IN TABLE I ARE THE ONLY QUALIFIED MANUFACTURERS.

1.3 PRIOR TO FINAL QUALIFICATION APPROVAL FOR ADDITIONAL SOURCES, MICROCIRCUITS SUPPLIED TO THIS DRAWING SHALL DEMONSTRATE SATISFACTORY PERFORMANCE IN THE ACTURAL APPLICATIONS.

2. PHYSICAL AND MECHANICAL CHARACTERISTICS.
PHYSICAL DIMENSIONS AND TERMINAL CONNECTIONS SHALL BE IN ACCORDANCE WITH FIGURES 1 AND 2, AND THE MECHANICAL CHARACTERISTICS AS REQUIRED IN Y125A18.0

DWN	SEE SH 1	SIZE A		DWG NO A 5 8 4 A Y Y Y	REV
ISSUED	SEE SH 1				SHEET

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3. ELECTRICAL CHARACTERISTICS.

3.1 ABSOLUTE MAXIMUM RATINGS.

3.1.1 TEMPERATURE RANGE.

3.1.1.1 OPERATING, T_C (MOUNTING SURFACE) ___ -55 TO +125 DEGREES C

3.1.1.2 STORAGE, T_{STG} _____ -65 TO +150 DEGREES C

3.1.2 CASE TEMPERATURE (MOUNTING SURFACE) T_C _____ +125 DEGREES C

3.1.2.1 CASE TEMPERATURE GRADIENT:
THE TEMPERATURE GRADIENT ACROSS THE MODULE BASE DURING MAXIMUM POWER DISSIPATION SHALL NOT EXCEED 15 DEGREES C.

3.1.3 JUNCTION TEMPERATURE, T_J _____ +130 DEGREES C

3.1.4 SUPPLY VOLTAGES:

3.1.4.1 +5 VOLT LINE _____ 7 VOLTS

3.1.4.2 POWER CONDITIONER HIGH LINE:

3.1.4.2.1 NO LOADS CONNECTED _____ 40 VOLTS

3.1.4.2.2 NOMINAL LOADS, D11=1 _____ +9.8 VOLTS

3.1.4.2.3 NOMINAL LOADS, D11=0 _____ +19.8 VOLTS

3.1.5 SIGNAL VOLTAGES:

3.1.5.1 480 HERTZ LINES _____ 5.5 VOLTS

3.1.5.2 D8, D11, D12 LINES _____ 5.5 VOLTS

3.2 ELECTRICAL PERFORMANCE CHARACTERISTICS:
THE FOLLOWING ELECTRICAL PERFORMANCE CHARACTERISTICS APPLY FOR THE CIRCUIT CONNECTED IN ACCORDANCE WITH FIGURE 5, WITH SUPPLY VOLTAGES OF 8.175 VOLTS DC, 16.5 VOLT DC AND 5 ±0.5 VOLTS DC WITH MAXIMUM SUPPLY RIPPLE OF 0.5 VOLT PEAK TO PEAK FOR FREQUENCY OF 30 HERTZ TO 1 MEGAHERTZ. PERFORMANCE CHARACTERISTICS SPECIFIED IN TABLE V APPLY OVER THE FULL OPERATING CASE TEMPERATURE RANGE OF -55 TO +125 DEGREES C.

3.2.1 INPUT CHARACTERISTICS:
FOUR 480 HERTZ SQUARE WAVE SIGNALS, EACH CAPABLE OF DRIVING TWO DTL LOADS, AT REFERENCE ANGLES OF 0, 90, 180, AND 270 DEGREES ARE NEEDED TO INSURE THE SPECIFIED CIRCUIT PERFORMANCE. THESE SIGNALS MAY BE GENERATED IN ACCORDANCE WITH FIGURE 4.

3.2.2 FAILURE MODE:

3.2.2.1 SHORT CIRCUIT BETWEEN ANY OUTPUT LINES (L1, L2, L3, L4, L5) OR ANY OUTPUT LINE AND GROUND, OR POWER SUPPLY.

3.3 TERMS, DEFINITIONS AND SYMBOLS:
TERMS, DEFINITIONS AND SYMBOLS SHALL BE IN ACCORDANCE WITH MIL-M-38510 AND AS FOLLOWS:

SYMBOL	DEFINITION
V_{O1}	OUTPUT VOLTAGE (LOW VOLTAGE MODE) MEASURED BETWEEN THE OUTPUT TERMINALS SPECIFIED.
V_{O2}	OUTPUT VOLTAGE (HIGH VOLTAGE MODE) MEASURED BETWEEN THE OUTPUT TERMINALS SPECIFIED
ΔV_{O1}	OUTPUT VOLTAGE STABILITY (LOW VOLTAGE MODE). FOR TABLE III, THE DIFFERENCE BETWEEN THE MEASURED VALUE OF V_{O1} IN SUBGROUP 4, AND V_{O1} IN THE SUBGROUP BEING TESTED (DRIFT LIMITS MUST BE DETERMINED WITH CONSTANT POWER SUPPLY VOLTAGE _ SUBGROUPS 4, 5, 6)
V_{OS}	OUTPUT OFFSET VOLTAGE, DC COMPONENT OF THE OUTPUT SQUARE WAVE, MEASURED BETWEEN TERMINALS SPECIFIED
T_{rf}	THE TIME REQUIRED FOR THE OUTPUT SQUARE WAVE TO GO FROM 90 PERCENT OF EITHER OF ITS LEVELS, TO 90 PERCENT OF THE OTHER
I_S	CURRENT SPIKES ON THE POWER CONDITIONER HIGH LINE AS SHOWN IN FIGURE 5.
f_1	THE MINIMUM INPUT FREQUENCY REQUIRED TO INHIBIT THE LOSS OF CLOCK PROTECTION CIRCUIT
TEST1	A TEST TO ASSURE CORRECT OPERATION OF THE LOSS OF CLOCK PROTECTION CIRCUIT
TEST2	A TEST TO ASSURE CORRECT OPERATION OF THE LOSS OF +5 VOLT POWER PROTECTION CIRCUIT
T_A	AMBIENT TEMPERATURE
T_C	CASE TEMPERATURE, MOUNTING SURFACE
T_J	JUNCTION TEMPERATURE
$P_{DISS(S)}$	HYBRID MODULE POWER DISSIPATION (START MODE)
$P_{DISS(R)}$	HYBRID MODULE POWER DISSIPATION (RUN MODE)
$I_{P.S.}$	POWER SUPPLY CURRENT DRAIN

4. ENVIRONMENTAL CONDITIONS.
IN ACCORDANCE WITH THE REQUIREMENTS OF Y125A18.0 EXCEPT AS MODIFIED OR AMENDED HEREIN.

5. QUALITY ASSURANCE PROVISIONS.
IN ACCORDANCE WITH THE REQUIREMENTS OF Y125A18.0 EXCEPT AS MODIFIED OR AMENDED HEREIN.

5.1 SCREENING.
ALL CIRCUITS SHALL BE SCREENED IN ACCORDANCE WITH Y125A18.0

A. BURN-IN CONDITIONS.

1. CIRCUIT: FIGURE 4.

2. T_C = +125 DEGREES C. (MOUNTING SURFACE)

B. ELECTRICAL PARAMETERS. SUBGROUPS 1, 2, 3 AND 4 OF TABLE VI.

5.2 GROUP A INSPECTION.
CIRCUITS SHALL BE SUBJECTED TO GROUP A INSPECTION, TABLE VI, ON A LOT SAMPLE BASIS TO AN LTPD OF 15.

5.3 GROUPS B, C AND D INSPECTIONS.
INSPECTIONS FOR GROUPS B, C AND D SHALL CONSIST OF THE TESTS DESCRIBED IN Y125A18.0 AND AS FOLLOWS:

A. OPERATING LIFE CONDITIONS.

1. CIRCUIT: FIGURE 4.

2. T_C = +125 DEGREES C. (MOUNTING SURFACE)

B. END POINT ELECTRICAL PARAMETERS. SUBGROUPS 1, 2, 3 AND 4 OF TABLE VI.

6. PREPARATION FOR DELIVERY.
IN ACCORDANCE WITH THE REQUIREMENTS OF Y125A18.0

DWN	SEE SH 1	SIZE A		DWG NO A584AYYY	REV
ISSUED	SEE SH 1	SCALE NONE		SHEET 24	

APPENDIX C

DESTRUCTIVE BOND PULL TEST PROGRAM

APPENDIX C

DESTRUCTIVE BOND PULL TEST PROGRAM

C.1 Computer Program used for Wirebond Pull Test described in Section 3.2.

```
20 D$ =  CHR$ (4):L$ =  CHR$ (12)
30 Q$ =  CHR$ (17):J$ =  CHR$ (10)
70  TEXT : PRINT D$;"PR#"4: POKE  - 12528,7: POKE  - 12531,20: PRINT
    D$;"PR#"0: PRINT
80  HOME : DIM B(500),Y(500),D(2400),X(250)
85 R = 0:N = 1:P = 0:S = 0:T = 0
90  VTAB 6
91  PR# 4: PRINT  TAB( 27)"DESTRUCTIVE BOND PULL TEST": PRINT  TAB(
    31)"SKD COMPONENTS LAB"
92  PRINT J$;"": PR# 0:R = R + 6
100  PRINT  TAB( 4)"THIS PROGRAM HAS BEEN WRITTEN TO AID IN THE DE
    STRUCTIVE TESTING OF LEAD BOND WIRES. AFTER ENTERING YOUR NAM
    E AND DATAASKED FOR, THE CURSOR WILL PROMPT YOU  FOR ADDITIO
    NAL INFORMATION. AFTER PULL-"
110  PRINT "ING THE BOND, ENTER A FAILURE OR DIRECT-IONAL CODE. TH
    E CODE AND FORCE WILL THEN BE PRINTED. THE CODES ARE LISTED I
    N THE FOLLOWING TABLE.
120  VTAB 24: PRINT  TAB( 8)"PRESS SPACE BAR TO CONT..": GET ANS$
130  HOME
140  PRINT  TAB( 8)"0 - CLEAR MPIII
150  PRINT  TAB( 8)"1 - WIRE BREAK AT BALL NECKDOWN": PRINT  TAB(
    12)"PT.": PRINT  TAB( 8)"2 - WIRE BREAK AT OTHER THAN NECK": VTAB
    5: PRINT  TAB( 12)"DOWN"
160  PRINT  TAB( 8)"3 - FAILURE IN BOND AT DIE": PRINT  TAB( 8)"4
    - FAILURE IN BOND AT OTHER THAN"
170  VTAB 8: PRINT  TAB( 12)"DIE": PRINT  TAB( 8)"5 - LIFTED METAL
    LIZATION FROM DIE": VTAB 10: PRINT  TAB( 8)"6 - LIFTED METALL
    IZATION FROM"
180  PRINT  TAB( 12)"OTHER THAN DIE": PRINT  TAB( 8)"7 - FRACTURE
    OF DIE": PRINT  TAB( 8)"8 - FRACTURE OF SUBSTRATE"
190  PRINT  TAB( 8)"9 - WIRE BREAK AT WEDGE NECKDOWN": PRINT  TAB(
    12)"PT.": PRINT  TAB( 7)"10 - NEXT LEAD"
200  PRINT  TAB( 7)"11 - NEXT DEVICE": PRINT  TAB( 7)"12 - GO BACK
     ONE LEAD": PRINT  TAB( 7)"14 - GO BACK ONE DEVICE"
210  VTAB 23: PRINT  TAB( 8)"PRESS SPACE BAR TO CONT....": GET ANS
    $
250  HOME
260  HOME : INPUT "PLEASE ENTER THE UNIT PART NUMBER  ";A$
270  INPUT "PLEASE ENTER THE LOT IDENTIFIER  ";T$
280  INPUT "PLEASE ENTER YOUR NAME  ";B$
290  INPUT "PLEASE ENTER THE DATE  ";C$
```

```
291  INPUT "PLEASE ENTER THE WIRE TYPE  ";E$
292  INPUT "PLEASE ENTER THE WIRE SIZE(MILS)  ";F$
295  INPUT "ENTER ANY SPECIAL CONDITIONS  ";S$
300  VTAB 20: INPUT "DO YOU WISH TO CHANGE ANYTHING (Y:N) ?";AN$
305  IF AN$ = "Y" THEN  GOTO 250
306  IF AN$ = "N" THEN  GOTO 310
307  GOTO 300
310  HOME : PR# 4: PRINT  TAB( 24)"PART NUMBER - "A$
320  PRINT  TAB( 21)"LOT IDENTIFIER - "T$
330  PRINT  TAB( 31)"NAME - "B$
340  PRINT  TAB( 31)"DATE - "C$
342  PRINT  TAB( 31)"WIRE - "F$" MIL "E$
345  PRINT  TAB( 17)"SPECIAL CONDITIONS - "S$
350  PRINT J$;"": PR# 0:R = R + 8
352  HOME : INPUT "WOULD YOU LIKE THE FAILURE CODE TABLE   PRINTED
      ?(Y:N)";AN$
356  IF AN$ = "Y" THEN  GOSUB 6600: GOTO 360
357  IF AN$ = "N" THEN  GOTO 360
358  GOTO 352
360  HOME : INPUT "DO YOU WANT TO RETRIEVE ANY DATA ?(Y:N)";AN$
362  IF AN$ = "Y" THEN  GOSUB 10100: GOTO 370
364  IF AN$ = "N" THEN  GOTO 370
366  GOTO 360
370  CALL 38320: REM   CLEAR MPIII
372  HOME : INPUT "ARE YOU PULLING ANY BONDS ? (Y:N) ";A$
373  IF A$ = "Y" THEN  GOTO 380
374  IF A$ = "N" THEN  GOTO 644
375  GOTO 372
380  PR# 4: PRINT  TAB( 12)"FORCE(GRAMS)"; SPC( 5);"FAILURE CODE":
      PRINT J$;"": PR# 0:R = R + 3
390  HOME : PRINT "ARE YOU PULLING ANY WIRES ON I'C'S?": PRINT  TAB(
     10)"1=YES": PRINT  TAB( 10)"0=NO"
400  INPUT A$
410  IF A$ = "1" THEN  HOME : GOTO 1000
420  IF A$ = "0" THEN  GOTO 440
430  PRINT "TRY AGAIN": GOTO 390
440  HOME : PRINT "ARE YOU PULLING ANY WIRES ON TRANSISTORS?": PRINT
      TAB( 10)"1=YES": PRINT  TAB( 10)"0=NO"
450  INPUT A$
460  IF A$ = "1" THEN  HOME : GOTO 2000
470  IF A$ = "0" THEN  GOTO 490
480  PRINT "TRY AGAIN": GOTO 450
490  HOME : PRINT "ARE YOU PULLING ANY WIRES ON DIODES?": PRINT  TAB(
     10)"1=YES": PRINT  TAB( 10)"0=NO
500  INPUT A$
510  IF A$ = "1" THEN  HOME : GOTO 3000
520  IF A$ = "0" THEN  GOTO 540
```

```
530  PRINT "TRY AGAIN": GOTO 500
540  HOME : PRINT "ARE YOU PULLING ANY WIRES ON RESISTORS?": PRINT
      TAB( 10)"1=YES": PRINT  TAB( 10)"0=NO"
550  INPUT A$
560  IF A$ = "1" THEN  HOME : GOTO 4000
570  IF A$ = "0" THEN  GOTO 590
580  PRINT "TRY AGAIN": GOTO 550
590  HOME : PRINT "ARE YOU PULLING ANY WIRES ON CAPACITORS?": PRINT
      TAB( 10)"1=YES": PRINT  TAB( 10)"0=NO"
600  INPUT A$
610  IF A$ = "1" THEN  HOME : GOTO 5000
620  IF A$ = "0" THEN  GOTO 632
630  PRINT "TRY AGAIN": GOTO 600
632  HOME : PRINT "ARE YOU PULLING ANY OTHER BOND WIRES ?": PRINT
      TAB( 10)"1 = YES": PRINT  TAB( 10)"0 = NO"
636  INPUT A$
638  IF A$ = "1" THEN  HOME : GOTO 6000
640  IF A$ = "0" THEN  GOTO 644
642  PRINT "TRY AGAIN ": GOTO 636
644  HOME :X =  FRE (0)
650  HTAB 8: PRINT "THIS IS THE END OF THE CURRENT    PROGRAM.IF Y
     OU WOULD LIKE TO REDO ONE     AREA,TYPE IN A NUMBER FROM THE
     LIST."
660  PRINT  TAB( 10)"I'C'S=1  ": PRINT  TAB( 4)"TRANSISTORS=2  ": PRINT
      TAB( 9)"DIODES=3  ": PRINT  TAB( 6)"RESISTORS=4  ": PRINT  TAB(
     5)"CAPACITORS=5  ": PRINT  TAB( 12)"END=6  "
670  INPUT A$
680  IF A$ = "1" THEN  HOME : GOTO 390
690  IF A$ = "2" THEN  HOME : GOTO 440
700  IF A$ = "3" THEN  HOME : GOTO 490
710  IF A$ = "4" THEN  HOME : GOTO 540
720  IF A$ = "5" THEN  HOME : GOTO 590
730  IF A$ = "6" THEN  GOTO 740
740 N = N - 1
745  IF N = 0 THEN  GOTO 800
750 B =  SQR ((T - (U / (N))) / ((N) - 1)):C = S / (N):E = B * 100

755  PR# 4:R = R + 1
760  IF R > 64 THEN R =  INT (R - 64): FOR I = (64 + R) TO 67: PRINT
     : NEXT I: PRINT "--"; SPC( 37);"--": PRINT L$;"":R = 3
765  PRINT J$;""
770  PRINT  TAB( 15)"THE MEAN ="C: PRINT  TAB( 5)"STANDARD DEVIATI
     ON ="B: PRINT  TAB( 3)"% STANDARD DEVIATION ="E: PRINT "NUMBE
     R OF BONDS PULLED ="N
```

```
780 R = R + 5: PR# 0
790  GOSUB 7000
800  HOME : INPUT "DO YOU WANT TO STORE ANY DATA (Y:N) ";AN$
802  IF AN$ = "Y" THEN  GOSUB 10200: GOTO 820
804  IF AN$ = "N" THEN  GOTO 820
806  GOTO 800
820  PR# 4: PRINT  TAB( 6)"NUMBER OF FAILURES = "K: PRINT "MIN ALL
     OWABLE BOND STRENGTH = "M
825 R = R + 2
827  IF R > 39 THEN  FOR J = R TO 64: PRINT : NEXT J: PRINT "--"; SPC(
     37);"--": PRINT L$;"":R = 3
830  PR# 0
835  HOME : CALL 64477
840  PRINT "IF YOU WISH TO DO GRAPHICAL ANALYSIS ON THE DATA THEN
     TYPE 'RUN CURFIT'.": END
```

```
1000  PRINT  TAB( 8)"HOW MANY I'C'S ARE THERE?": INPUT A
1015  HOME : INPUT "WHAT DEVICE NUMBER ARE YOU STARTING     WITH ?
      ";0
1020  HOME : PRINT  TAB( 12)"FORCE(GRAMS)"; SPC( 5);"FAILURE CODE"

1040  FOR I = 0 TO A: FOR L = 1 TO 65
1050  CALL 38320: REM   CLEAR MPIII
1060  PRINT  TAB( 4)"U"I"-"L
1070  INPUT X
1080  IF X = 0 THEN  CALL 38320: GOTO 1070
1090  IF X <  = 9 THEN  GOTO 1150
1100  IF X = 10 THEN  GOTO 1270
1110  IF X = 11 THEN  GOTO 1275
1120  IF X = 12 THEN L = L - 1: GOTO 1060
1130  IF X = 14 THEN I = I - 1: GOTO 1060
1140  GOTO 1070
1150  CALL 38320
1160 Y = 10 *  PEEK (38347) +  PEEK (38348) + .1 *  PEEK (38349)
1170  PRINT  TAB( 14)Y; TAB( 34)X
1180 Y(N) = Y:N = N + 1:S = S + Y:T = T + Y ^ 2:U = S ^ 2
1224  PR# 4
1225  IF R > 61 THEN  FOR J = R TO 64: PRINT : NEXT J: PRINT "--";
      SPC( 37);"--": PRINT L$;"": PRINT  TAB( 12)"FORCE(GRAMS)"; SPC(
     5);"FAILURE CODE": PRINT J$:R = 6
1230  PRINT  TAB( 4)"U"I"-"L,Y,X: PR# 0:R = R + 1
1270  NEXT L
1275  PR# 4: PRINT : PR# 0:R = R + 1
1280  NEXT I
1290  PR# 4: PRINT J$;"": PR# 0:R = R + 1
1300  PRINT "YOU HAVE FINISHED THE PROGRAM FOR INTE- GRATED CIRCUI
     TS.PRESS ENTER TO CONTINUE. ": GET ANS$
1310  GOTO 440
```

```
2000  HOME : PRINT  TAB( 8)"HOW  MANY TRANSISTORS ARE THERE ?": INPUT
     A
2025  HOME : INPUT "WHAT DEVICE NUMBER ARE YOU STARTING     WITH ?
     ";O
2030  HOME : PRINT  TAB( 12)"FORCE(GRAMS)"; SPC( 5);"FAILURE CODE"

2050  FOR I = 0 TO A: FOR L = 1 TO 3
2060  CALL 38320
2070  IF L = 1 THEN  PRINT  TAB( 4)"Q"I"E"
2080  IF L = 2 THEN  PRINT  TAB( 4)"Q"I"B"
2090  IF L = 3 THEN  PRINT  TAB( 4)"Q"I"C"
2100  INPUT X
2110  IF X = 0 THEN  CALL 38320: GOTO 2100
2120  IF X <  = 9 THEN  GOTO 2180
2130  IF X = 10 THEN  GOTO 2340
2140  IF X = 11 THEN  GOTO 2345
2150  IF X = 12 THEN L = L - 1: GOTO 2060
2160  IF X = 14 THEN I = I - 1: GOTO 2060
2170  GOTO 2100
2180  CALL 38320
2190 Y = 10 *  PEEK (38347) +  PEEK (38348) + .1 *  PEEK (38349)
2200  PRINT  TAB( 14)Y; TAB( 34)X
2210 Y(N) = Y:N = N + 1:S = S + Y:T = T + Y ^ 2:U = S ^ 2
2260  PR# 4
2265  IF R > 61 THEN  FOR J = R TO 64: PRINT : NEXT J: PRINT "--";
     SPC( 37);"--": PRINT L$;"": PRINT  TAB( 12)"FORCE(GRAMS)"; SPC(
     5);"FAILURE CODE": PRINT J$:R = 6
2270  IF L = 1 THEN  PRINT  TAB( 4)"Q"I"E",Y,X: GOTO 2300
2280  IF L = 2 THEN  PRINT  TAB( 4)"Q"I"B",Y,X: GOTO 2300
2290  IF L = 3 THEN  PRINT  TAB( 4)"Q"I"C",Y,X
2300  PR# 0:R = R + 1
2340  NEXT L
2345  PR# 4: PRINT : PR# 0:R = R + 1
2350  NEXT I
2360  PR# 4: PRINT J$;"": PR# 0:R = R + 1
2370  PRINT "YOU HAVE FINISHED THE PROGRAM FOR TRAN- SISTORS.PRESS
     ENTER TO CONTINUE. ": GET ANS$
2380  GOTO 490
```

```
3000  HOME : PRINT  TAB( 8)"HOW MANY DIODES ARE THERE ?": INPUT A
3015  HOME : INPUT "WHAT DEVICE NUMBER ARE YOU STARTING     WITH ?
      ";O
3020  HOME : PRINT  TAB( 12)"FORCE(GRAMS)"; SPC( 5);"FAILURE CODE"

3040  FOR I = 0 TO A
3050  CALL 38320
3060  PRINT  TAB( 4)"CR"I
3070  INPUT X
3080  IF X = 0 THEN  CALL 38320: GOTO 3070
3090  IF X <  = 9 THEN  GOTO 3130
3100  IF X = 11 THEN  GOTO 3220
3110  IF X = 14 THEN I = I - 1: GOTO 3050
3120  GOTO 3070
3130  CALL 38320
3140 Y = 10 *  PEEK (38347) +  PEEK (38348) + .1 *  PEEK (38349)
3150  PRINT  TAB( 14)Y; TAB( 34)X
3160 Y(N) = Y:N = N + 1:S = S + Y:T = T + Y ^ 2:U = S ^ 2
3174  PR# 4
3175  IF R > 61 THEN  FOR J = R TO 64: PRINT : NEXT J: PRINT "--";
      SPC( 37);"--": PRINT L$;"": PRINT  TAB( 12)"FORCE(GRAMS)"; SPC(
     5);"FAILURE CODE": PRINT J$:R = 6: PR# 0
3180  PR# 4: PRINT  TAB( 4)"CR"I,Y,X: PR# 0
3185 R = R + 1
3220  NEXT I
3230  PR# 4: PRINT J$;"": PR# 0:R = R + 1
3240  PRINT "YOU HAVE FINISHED THE PROGRAM FOR DIODES PRESS  ENTER
      TO CONTINUE.": GET ANS$
3250  GOTO 540
```

```
4000  HOME : PRINT  TAB( 8)"HOW MANY RESISTORS ARE THERE ?": INPUT
    A
4015  HOME : INPUT "WHAT DEVICE NUMBER  ARE YOU STARTING     WITH
    ? ";O
4020  HOME : PRINT  TAB( 12)"FORCE(GRAMS)"; SPC( 5);"FAILURE CODE"

4040  FOR I = O TO A: FOR L = 1 TO 2
4050  CALL 38320
4060  IF L = 1 THEN  PRINT  TAB( 4)"R"I"-1"
4070  IF L = 2 THEN  PRINT  TAB( 4)"R"I"-2"
4080  INPUT X
4090  IF X = 0 THEN  CALL 38320: GOTO 4080
4100  IF X <  = 9 THEN  GOTO 4160
4110  IF X = 10 THEN  GOTO 4280
4120  IF X = 11 THEN  GOTO 4285
4130  IF X = 12 THEN L = L - 1: GOTO 4050
4140  IF X = 14 THEN I = I - 1: GOTO 4050
4150  GOTO 4080
4160  CALL 38320
4170 Y = 10 *  PEEK (38347) +  PEEK (38348) + .1 *  PEEK (38349)
4180  PRINT  TAB( 14)Y; TAB( 34)X
4190 Y(N) = Y:N = N + 1:S = S + Y:T = T + Y ^ 2:U = S ^ 2
4204  PR# 4
4205  IF R > 61 THEN  FOR J = R TO 64: PRINT : NEXT J: PRINT "--";
     SPC( 37);"--": PRINT L$;"": PRINT  TAB( 12)"FORCE(GRAMS)"; SPC(
    5);"FAILURE CODE": PRINT J$:R = 6: PR# 0
4210  PR# 4
4220  IF L = 1 THEN  PRINT  TAB( 4)"R"I"-1",Y,X: GOTO 4240
4230  IF L = 2 THEN  PRINT  TAB( 4)"R"I"-2",Y,X
4240  PR# 0:R = R + 1
4280  NEXT L
4285  PR# 4: PRINT : PR# 0:R = R + 1
4290  NEXT I
4295  PR# 4: PRINT J$;"": PR# 0:R = R + 1
4300  PRINT "YOU HAVE FINISHED THE PROGRAM FOR RE-   SISTORS.PRESS
      ENTER TO CONTINUE.": GET ANS$
4310  GOTO 590
```

```
5000  HOME : PRINT  TAB( 8)"HOW MANY CAPACITORS ARE THERE ?": INPUT
    A
5015  HOME : INPUT "WHAT DEVICE NUMBER ARE YOU STARTING     WITH ?
     ";0
5020  HOME : PRINT  TAB( 12)"FORCE(GRAMS)"; SPC( 5);"FAILURE CODE"

5040  FOR I = 0 TO A: FOR L = 1 TO 2
5050  CALL 38320
5060  IF L = 1 THEN  PRINT  TAB( 4)"C"I"-1"
5070  IF L = 2 THEN  PRINT  TAB( 4)"C"I"-2"
5080  INPUT X
5090  IF X = 0 THEN  CALL 38320: GOTO 5080
5100  IF X <  = 9 THEN  GOTO 5160
5110  IF X = 10 THEN  GOTO 5280
5120  IF X = 11 THEN  GOTO 5285
5130  IF X = 12 THEN L = L - 1: GOTO 5050
5140  IF X = 14 THEN I = I - 1: GOTO 5050
5150  GOTO 5080
5160  CALL 38320
5170 Y = 10 *  PEEK (38347) +  PEEK (38348) + .1 *  PEEK (38349)
5180  PRINT  TAB( 14)Y; TAB( 34)X
5190 Y(N) = Y:N = N + 1:S = S + Y:T = T + Y ^ 2:U = S ^ 2
5204  PR# 4
5205  IF R > 61 THEN  FOR J = R TO 64: PRINT : NEXT J: PRINT "--";
     SPC( 37);"--": PRINT L$;"": PRINT  TAB( 12)"FORCE(GRAMS)"; SPC(
    5);"FAILURE CODE": PRINT J$:R = 6
5220  IF L = 1 THEN  PRINT  TAB( 4)"C"I"-1",Y,X: GOTO 5240
5230  IF L = 2 THEN  PRINT  TAB( 4)"C"I"-2",Y,X
5240  PR# 0:R = R + 1
5280  NEXT L
5285  PR# 4: PRINT : PR# 0:R = R + 1
5290  NEXT I
5295  PR# 4: PRINT J$;"": PR# 0:R = R + 1
5300  PRINT "YOU HAVE FINISHED THE PROGRAM FOR CA-    PACITORS.PRE
    SS  ENTER TO CONTINUE.": GET ANS$
5310  GOTO 632
```

```
6000  HOME : PRINT "TO END THIS ROUTINE ENTER '20' AFTER THE PROMP
     T."6005
6010  INPUT "ENTER THE DESIGNATOR ";A$
6015  INPUT "WHAT LEAD # ARE YOU STARTING WITH ?";A
6020  HOME : PRINT  TAB( 12)"FORCE(GRAMS)"; SPC( 5);"FAILURE CODE"

6050  FOR I = A TO 100
6060  CALL 38320
6070  PRINT  TAB( 4)A$" - "I
6080  INPUT X
6090  IF X = 0 THEN  CALL 38320: GOTO 6080
6100  IF X <  = 9 THEN  GOTO 6140
6110  IF X = 10 THEN  GOTO 6250
6115  IF X = 11 THEN  PR# 4: PRINT : PR# 0:R = R + 1: GOTO 6010
6120  IF X = 12 THEN I = I - 1: GOTO 6070
6125  IF X = 20 THEN  GOTO 6270
6130  GOTO 6080
6140  CALL 38320
6150 Y = 10 *  PEEK (38347) +  PEEK (38348) + .1 *  PEEK (38349)
6160  PRINT  TAB( 14)Y; TAB( 34)X
6170 Y(N) = Y:N = N + 1:S = S + Y:T = T + Y ^ 2:U = S ^ 2
6189  PR# 4
6190  IF R > 61 THEN  FOR J = R TO 64: PRINT : NEXT J: PRINT "--";
      SPC( 37);"--": PRINT L$;"": PRINT  TAB( 12)"FORCE(GRAMS)"; SPC(
     5);"FAILURE CODE": PRINT J$:R = 6
6200  PRINT  TAB( 4)A$" - "I,Y,X: PR# 0
6210 R = R + 1
6250  NEXT I
6260  PR# 4: PRINT J$;"": PR# 0:R = R + 1
6270  GOTO 644
```

```
7000 M = N:U = N
7010 M =  INT (M / 2)
7020  IF M = 0 THEN  GOTO 7150
7030 J = 0:K = N - M
7040 I = J
7050 L = I + M
7060  IF Y(I) = Y(L) THEN  GOTO 7120
7070  IF Y(I) < Y(L) THEN  GOTO 7120
7080 P = Y(I):Y(I) = Y(L):Y(L) = P
7090 I = I - M
7100  IF I < 1 THEN  GOTO 7120
7110  GOTO 7050
7120 J = J + 1
7130  IF J > K THEN  GOTO 7010
7140  GOTO 7040
7150  CALL 64477: HOME
7170  IF G = 0 THEN K = 0: GOTO 7180
7180  GOSUB 9000
7190  RETURN
```

```
9000  PRINT "ENTER THE MIN ALLOWABLE BOND STRENGTH": INPUT M
9001  FOR I = 1 TO U: IF Y(I) < M THEN K = K + 1: NEXT I
9002  HOME : PRINT "PLEASE BE PATIENT.I'M SORTING DATA"
9010  FOR I = 1 TO 249: READ X(I): NEXT I
9040  FOR I = 1 TO U
9050  FOR S = 1 TO 207
9060  IF I / (U + 1) < X(S) THEN B(I) = S: GOTO 9100
9070  IF I / (U + 1) > .9768 THEN B(I) = 206: GOTO 9100
9080  NEXT S
9100  NEXT I
9102  FOR I = 1 TO U
9104  IF B(I) >  = 126 THEN B(I) = 0 + ((B(I) - 125) * .024): GOTO
     9110
9105  IF B(I) <  = 124 THEN B(I) = 0 - ((125 - B(I)) * .024): GOTO
     9110
9108  IF B(I) = 125 THEN B(I) = 0: GOTO 9110
9110  NEXT I
9115 D(0) = 2 * N
9116 L = 1
9120  FOR I = 1 TO N
9130 D(L) = B(I)
9140 D(L + 1) = Y(I)
9151 L = L + 2
9155  NEXT I
9156  GOSUB 10000
9160  RETURN
9200  DATA     1.48017E-03,1.57862E-03,1.7057E-03,1.8421E-03,1.988
     4E-03,2.1451E-03,2.3129E-03,2.4925E-03,2.6846E-03,2.89E-03,3.
     1095E-03,3.3492E-03,3.594E-03,3.8609E-03,4.1453E-03,4.448327E
     -3,4.771E-3,5.1143E-3,5.4795E-3,5.8677E-3,6.280E-3
9210  DATA  6.71797E-3,7.18258E-3,7.6753E-3,8.19753E-3,8.75073E-3,
     9.33638E-3,9.9560E-3,.010611,.01130,.01203,.0128,.0136,.0145,
     .0154,.0163,.0173,.0184,.0195,.0207,.0219
9220  DATA  .0232,.0245,.0259,.0274,.029,.0306,.0323,.0341,.0359,.
     0379,.0399,.042,.0442,.0465,.0489,.0513,.0539,.0566,.0594,.06
     23
9230  DATA  .0653,.0684,.0716,.0749,.0784,.082,.0856,.0895,.0934,.
     0975,.1017,.1060,.1105,.1151,.1198,.1247,.1297,.1348,.1401,.1
     455
9240  DATA   .1510,.1567,.162,.1685,.1746,.1809,.1873,.1938,.2004,
     .2072,.2142,.2212,.2284,.2358,.2432,.2508,.2585,.2663,.2742,.
     2823
9250  DATA  .2905,.2987,.3071,.3156,.3242,.3329,.3416,.3505,.3594,
     .3684,.3775,.3867,.3959,.4052,.4145,.4239,.4333,.4427,.4522,.
     4618
9260  DATA   .4713,.4808,.4904,.5,.5096,.5191,.5287,.5382,.5477,.5
     573,.5667,.5761,.5855,.5948,.6041,.6133,.6225,.6316,.6406,.64
     95
```

```
9270  DATA  .6584,.6671,.6758,.6844,.6929,.7012,.7095,.7177,.7257,
     .7337,.7415,.7492,.7568,.7642,.7716,.7787,.7858,.7927,.7995
9280  DATA  .8062,.8127,.8191,.8254,.8315,.8374,.8433,.849,.8545,.
     8599,.8652,.8703,.8753,.8802,.8849,.8895,.894,.8983,.9025,.90
     66,.9105
9290  DATA  .9143,.9180,.9216,.9251,,9284,.9316,.9347,.9377,.9406,
     .9434,.9461,.9487,.9511,.9535,.9558,.9580,.9601,.9621,.9641,.
     9659
9300  DATA    .9677,.9694,.9710,.9726,.9740,.9755,.9768,.9781,.979
     3,.9805,.9816,.9826,.9837,.9846,.9855,.9864,.9872,.988,.9887,
     .9894
9310  DATA  .9900,.9907,.9912,.9918,.9923,.9928,.9933,.9937,.9941,
     .9945,.9949,.9952,.9955,.9958,.9961,.9964,.9966,.9969,.9971,.
     9973
9320  DATA  .9975,.9977,,.,9978,.9980,.9981,.9984,.9985
```

```
10000  REM  DATA STORAGE ROUTINE
10010  PRINT D$;"OPEN TEMP"
10020  PRINT D$;"DELETE TEMP"
10030  PRINT D$;"OPEN TEMP"
10040  PRINT D$;"WRITE TEMP"
10050  FOR I = 0 TO 2 * N: PRINT D(I): NEXT I
10060  PRINT D$;"CLOSE TEMP"
10070  RETURN
10100  REM   DATA RETRIEVAL ROUTINE
10110  PRINT D$;"OPEN DATA ONE": PRINT D$;"READ DATA ONE"
10120  INPUT G: INPUT T: INPUT V: INPUT S: INPUT N
10130  FOR I = 1 TO N: INPUT Y(I): NEXT I
10140 N = N + 1: PRINT D$;"CLOSE DATA ONE"
10150  RETURN
10200  REM  DATA STORAGE ROUTINE
10210  PRINT D$;"OPEN DATA ONE": PRINT D$;"DELETE DATA ONE": PRINT
     D$;"CLOSE DATA ONE"
10220  PRINT D$;"OPEN DATA ONE": PRINT D$;"WRITE DATA ONE"
10230  PRINT G: PRINT T: PRINT V: PRINT S: PRINT N
10240  FOR I = 0 TO N: PRINT Y(I): NEXT I
10250  PRINT D$;"CLOSE DATA ONE": RETURN
```

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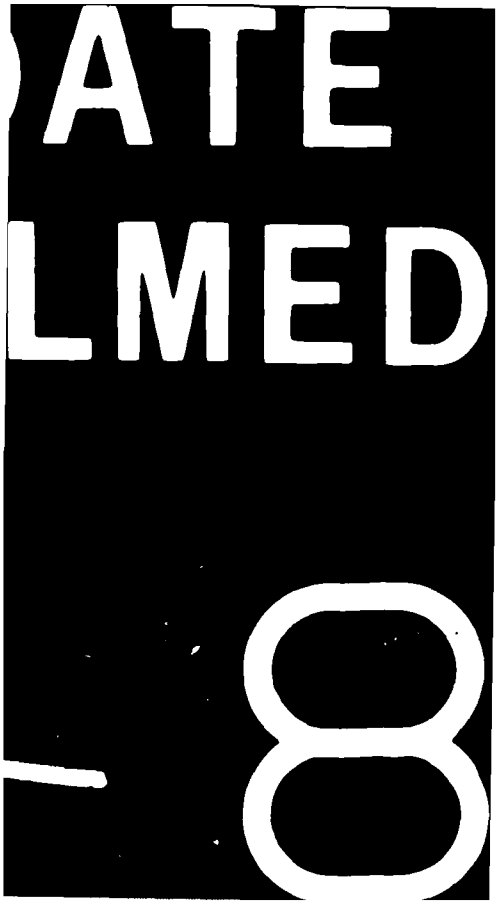
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